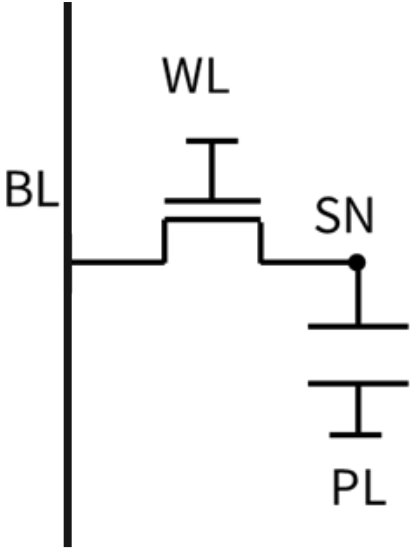
Water Bottle Memory

Has water – state “1”
No water – state “0”

How can you tell if there is water or not?

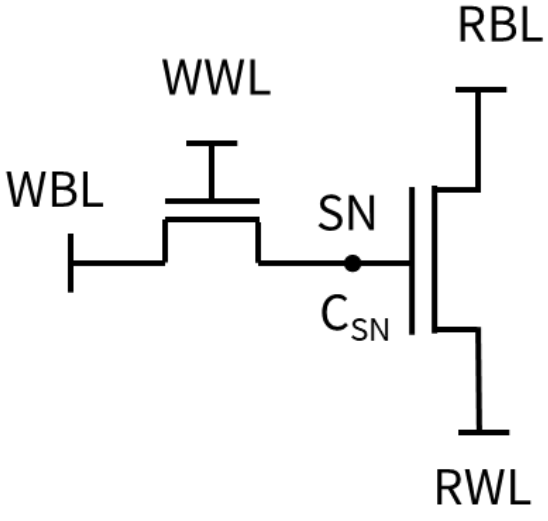
Water Bottle Memory

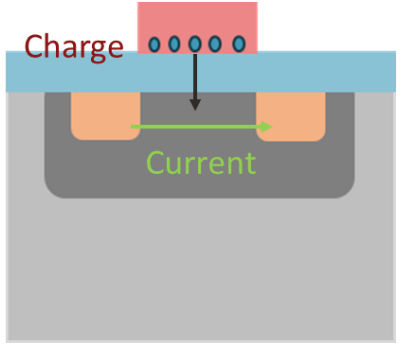
1T1C DRAM



Pour out water to BL tank

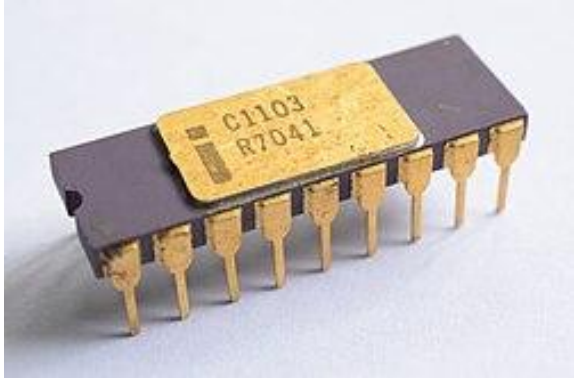
2T Gain Cell

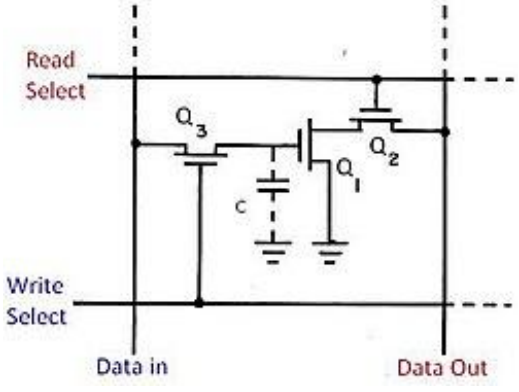




Measuring the weight of water

Intel 1103: First Commercial DRAM IC (1970)

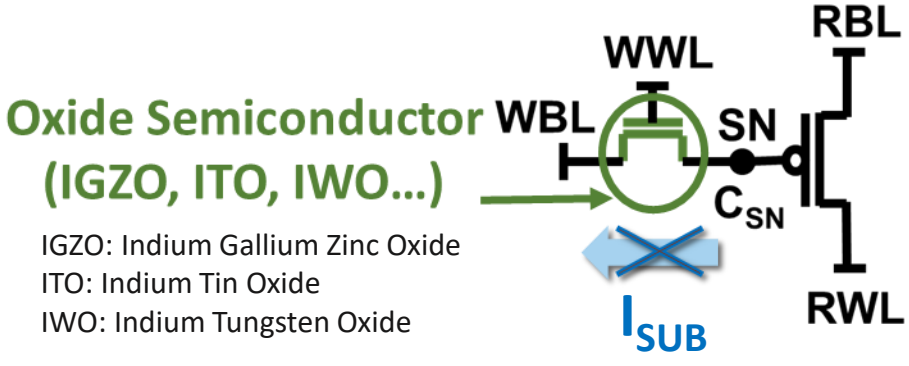


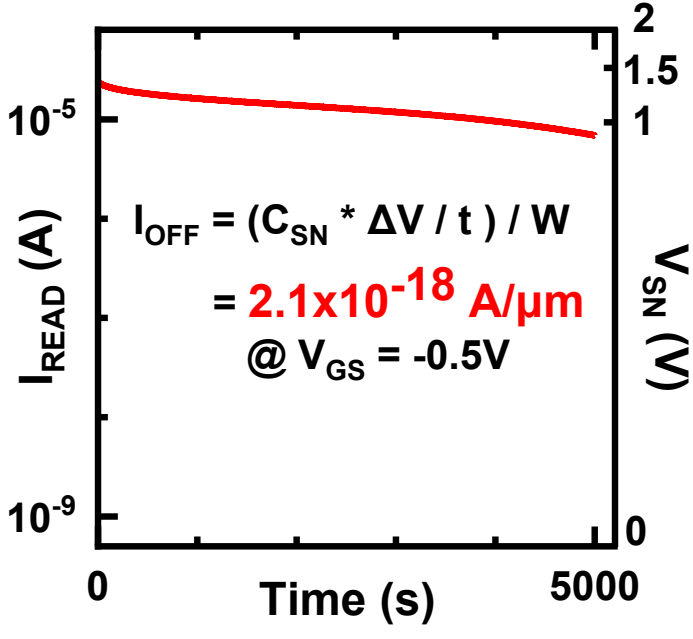


https://en.wikipedia.org/wiki/Intel_1103

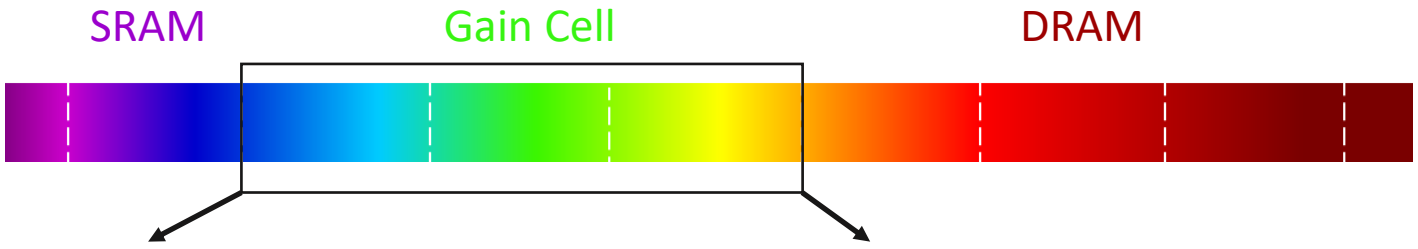
Oxide Semiconductor

wide bandgap → low leakage → long retention



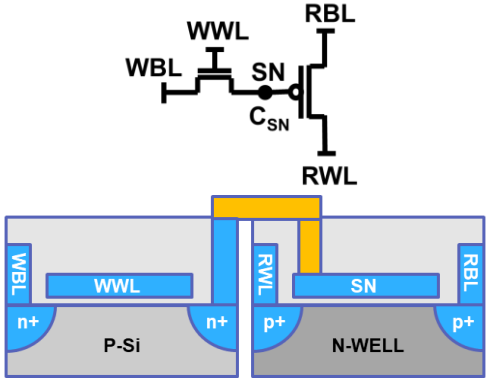


Gain Cell: SRAM-like pseudo-DRAM



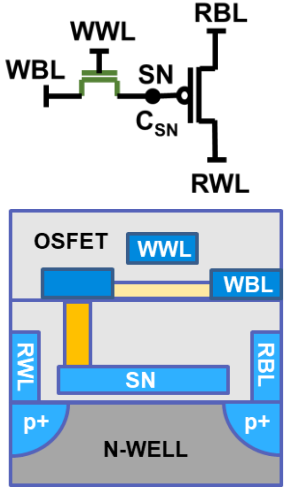
Si-Si gain cell

IEDM'25 28-8 (S. Liu)



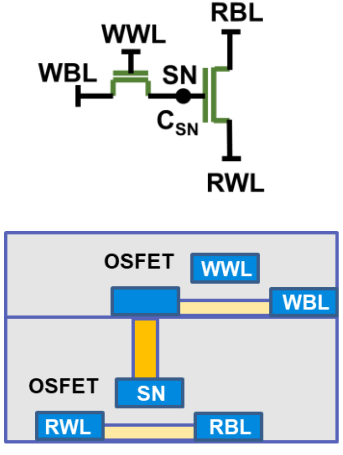
OS-Si hybrid gain cell

VLSI'24, IEDM'25 29-5 (S. Liu)

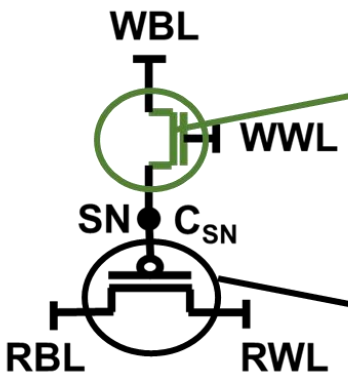


OS-OS gain cell

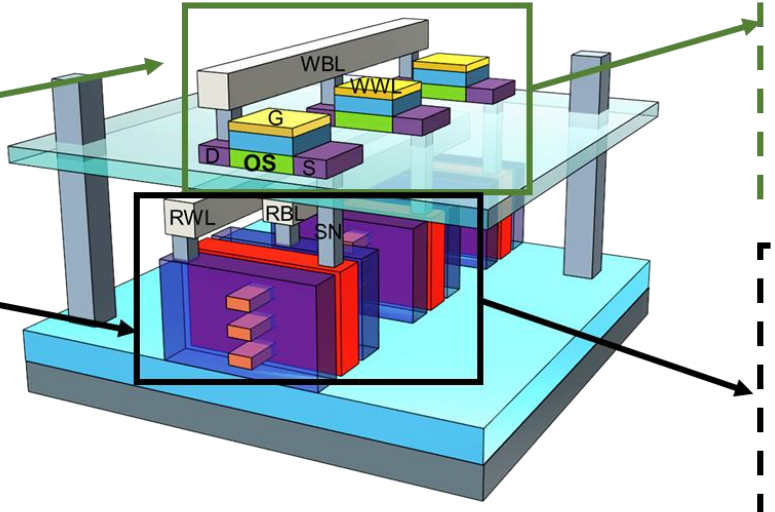
VLSI'23, IEDM'23 (S. Liu)



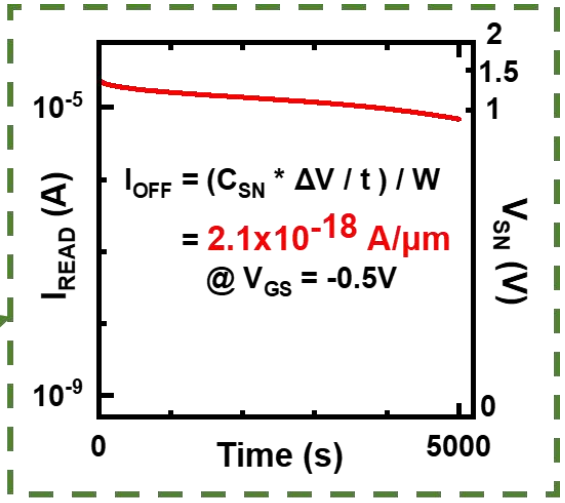
Hybrid Gain Cell

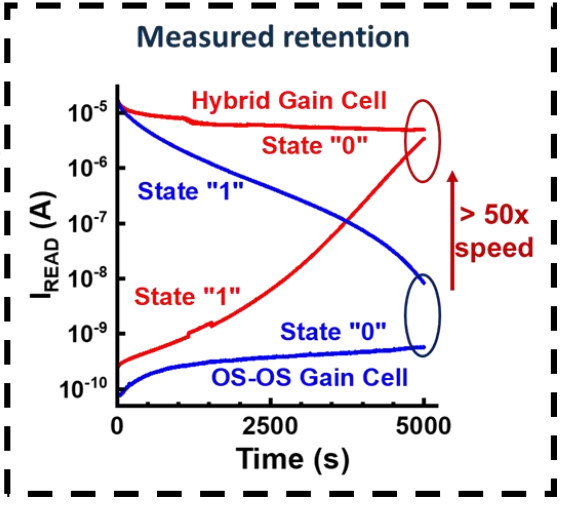


Oxide Semi. write transistor:
- ✓ Low leakage current
- ✓ Logic compatible

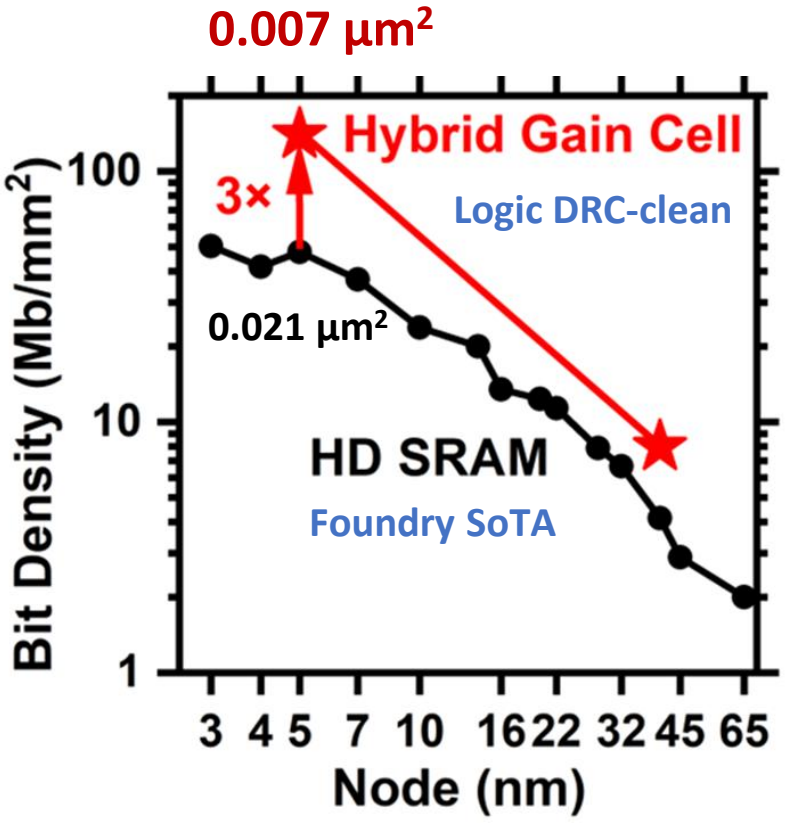


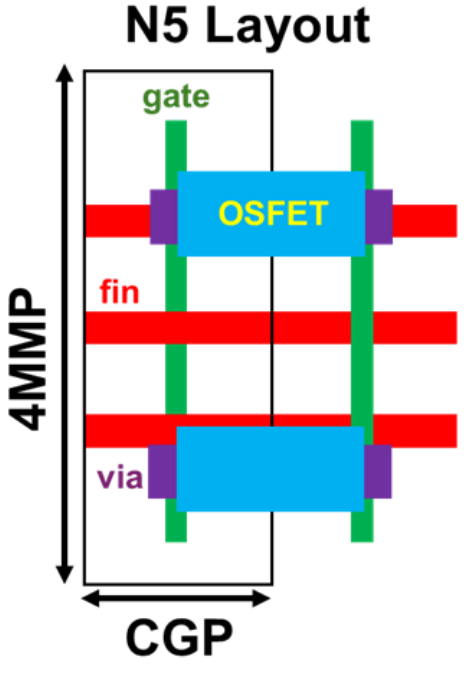
Si PMOS read transistor:
- ✓ High Mobility (Si)
- ✓ Coupling Offset (p-type)
- ✓ State Mapping (p-type)
- ✓ Bias Reliability (Si)





Hybrid Gain Cell Array Density 3× of HD SRAM

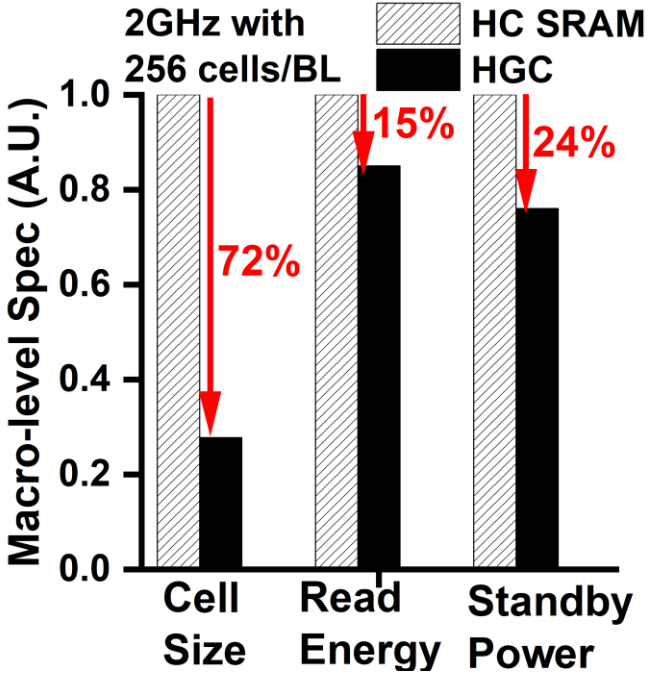




Collaboration with Nvidia

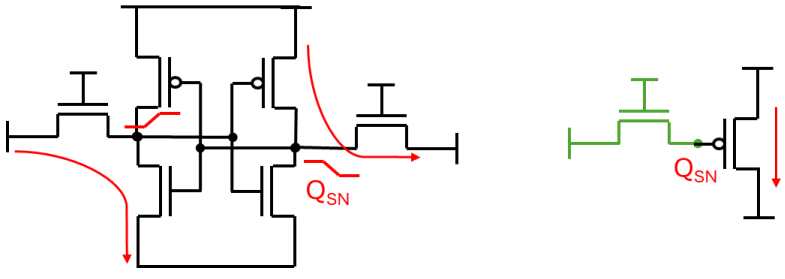
Shuhan Liu,… H.-S. P. Wong, *IEDM 2025 29-5*.

Hybrid Gain Cell Macro Lower Energy than SRAM



Collaboration with Nvidia

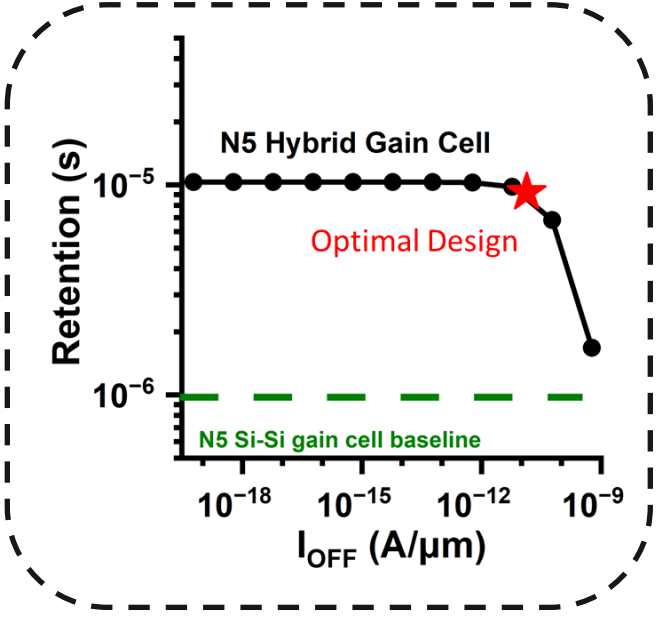
Lower Read Energy than SRAM



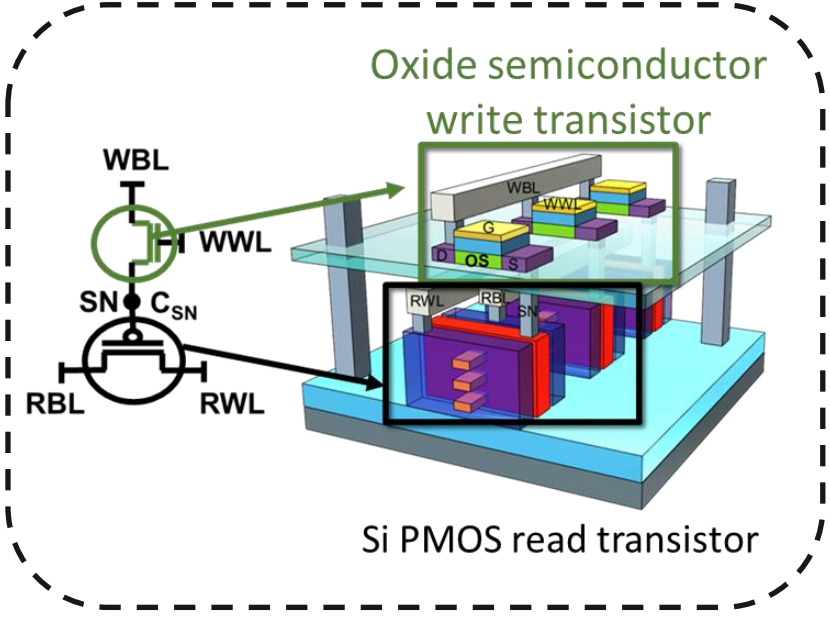
HC SRAM: high-current SRAM
HGC: hybrid gain cell (OS-Si)

Limitation of Hybrid Gain Cell

Retention limited by gate leakage of Si read transistor



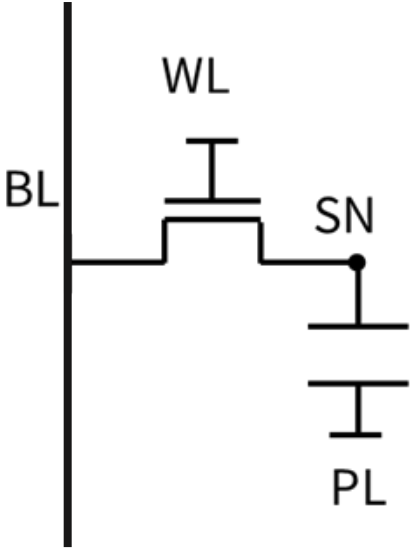
Not 3D-scalable



Shuhan Liu,… H.-S. P. Wong, *IEDM 29-5*, 2025.

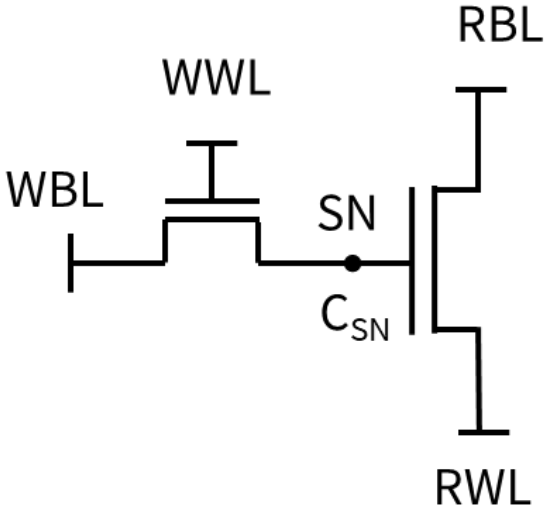
Water Bottle Memory

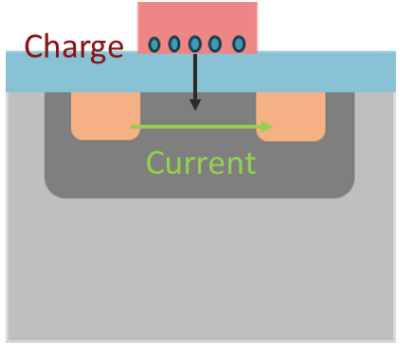
1T1C DRAM



Pour out water to BL tank

2T Gain Cell

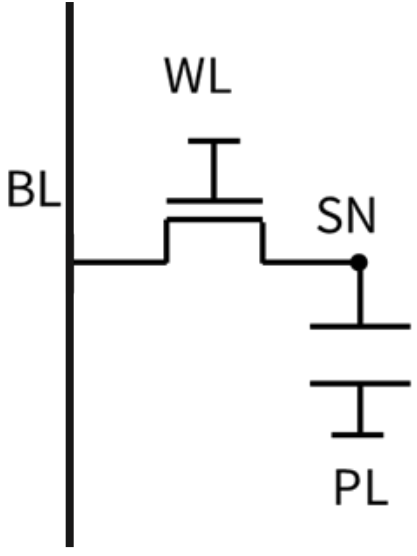




Measuring the weight of water

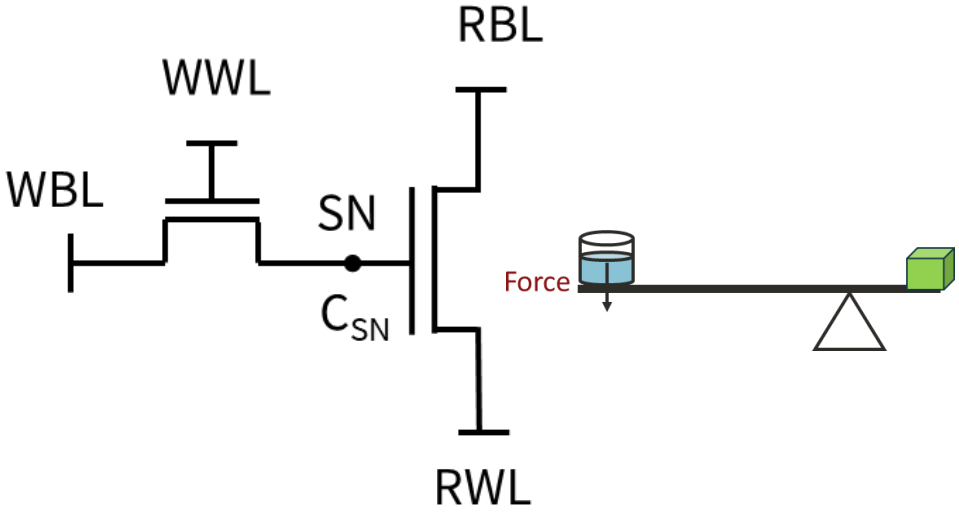
Water Cup Memory (On-chip Small Capacitor)

1T1C eDRAM



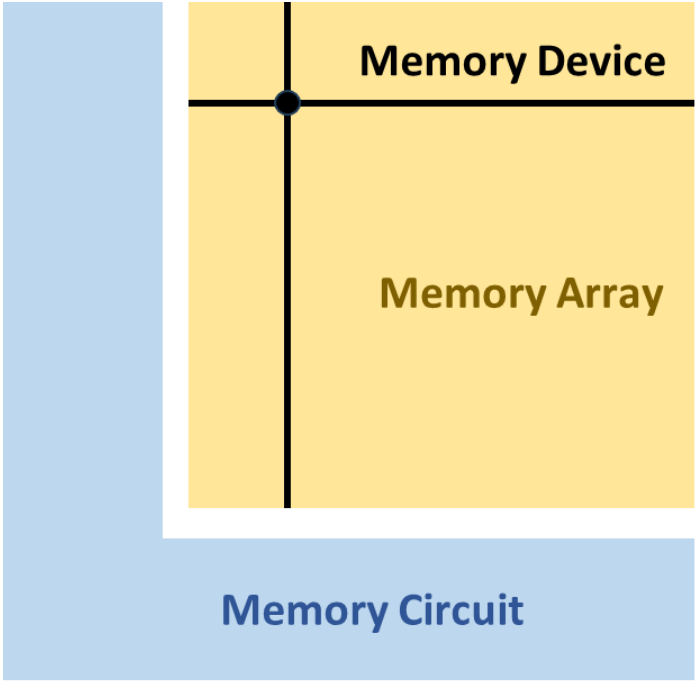
Pour out water to BL tank
-> Smaller tank (shorter BL)

2T Gain Cell

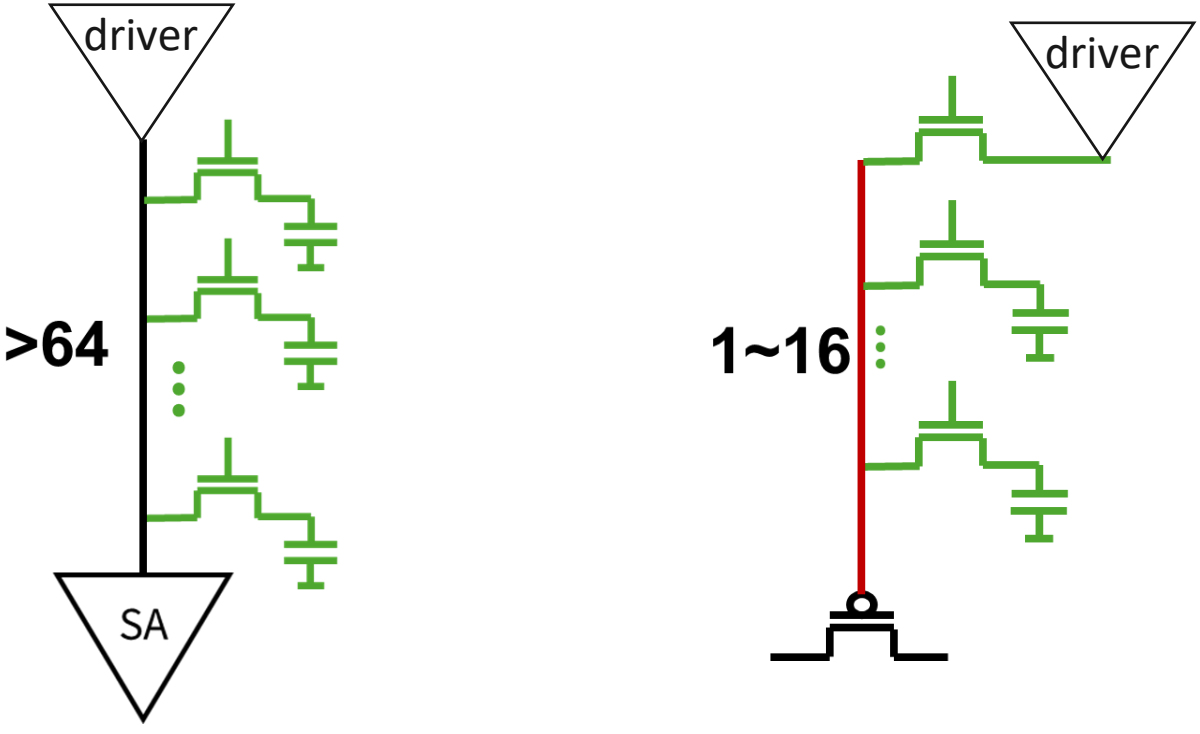


Measuring the weight of water
-> Increase the amplification (Si higher gain)

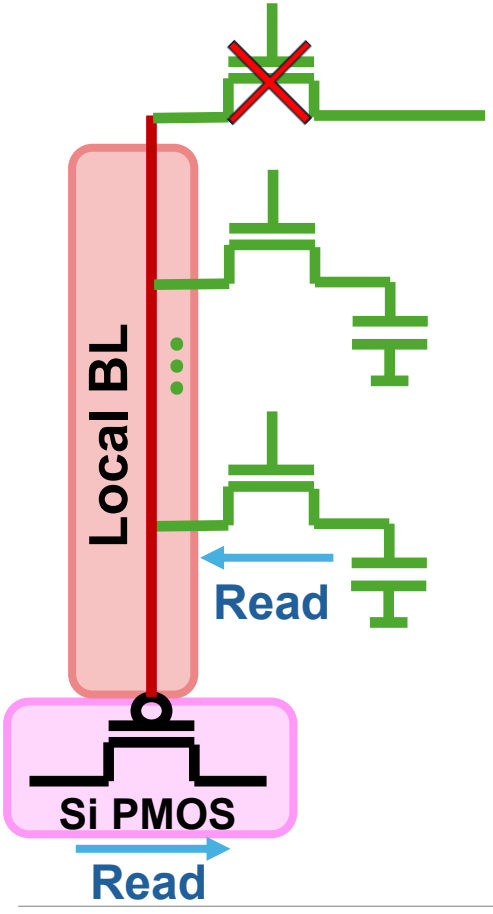
Small Granularity: Lower Area Efficiency



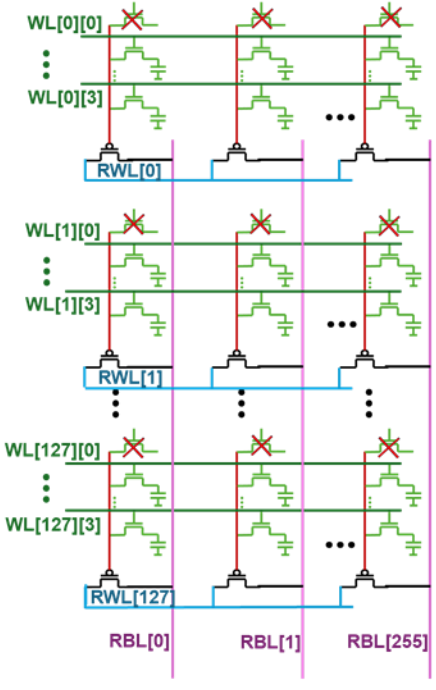
Amp Cell: Area Efficient eDRAM



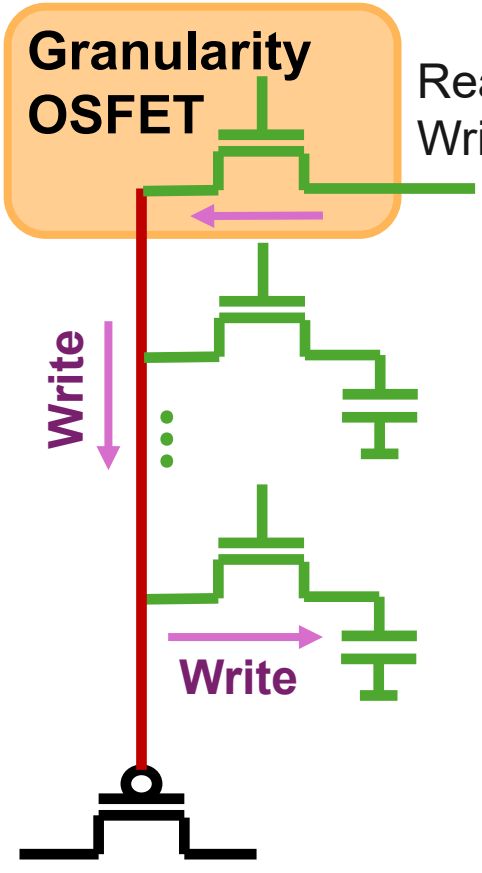
Local Amplification Read



Local Charge Share (4 cells/LBL) +
Read Amplification (128 cells/RBL)

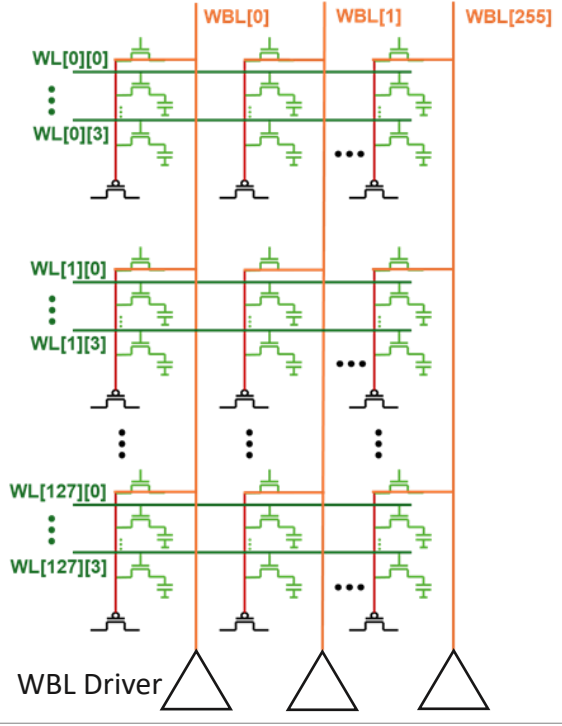


Global Write



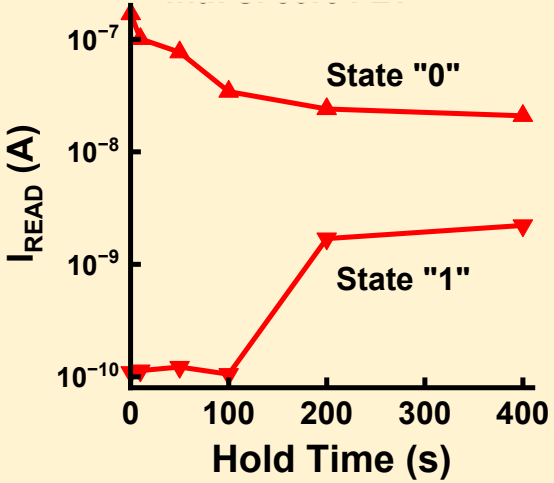
Read: Small Granularity Optimized for Speed
Write: Large Granularity Optimized for Area Efficiency

512 cells/WBL sharing one driver

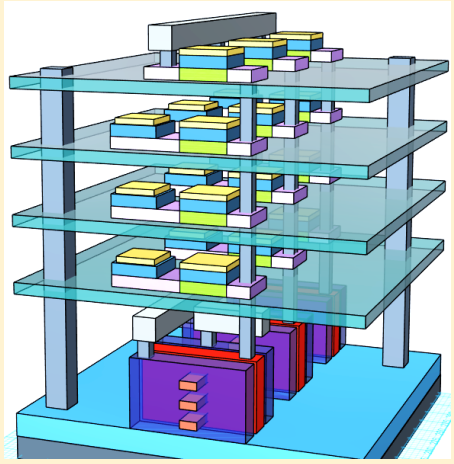


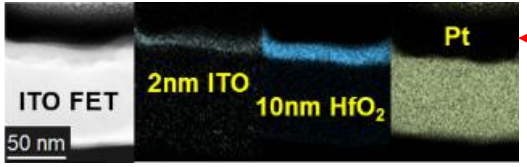
Amp Cell on N40 CMOS+X Chip

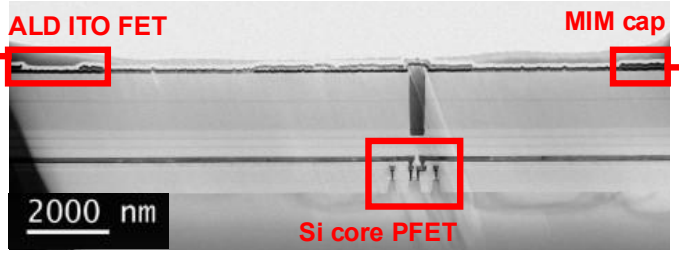
Retention > 5× with same Si core transistor

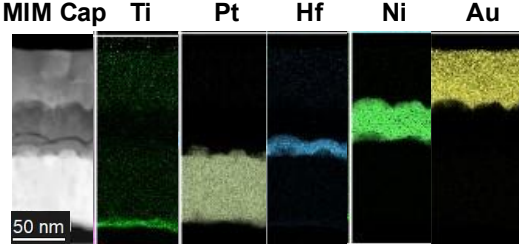


3D-scalable and logic-compatible









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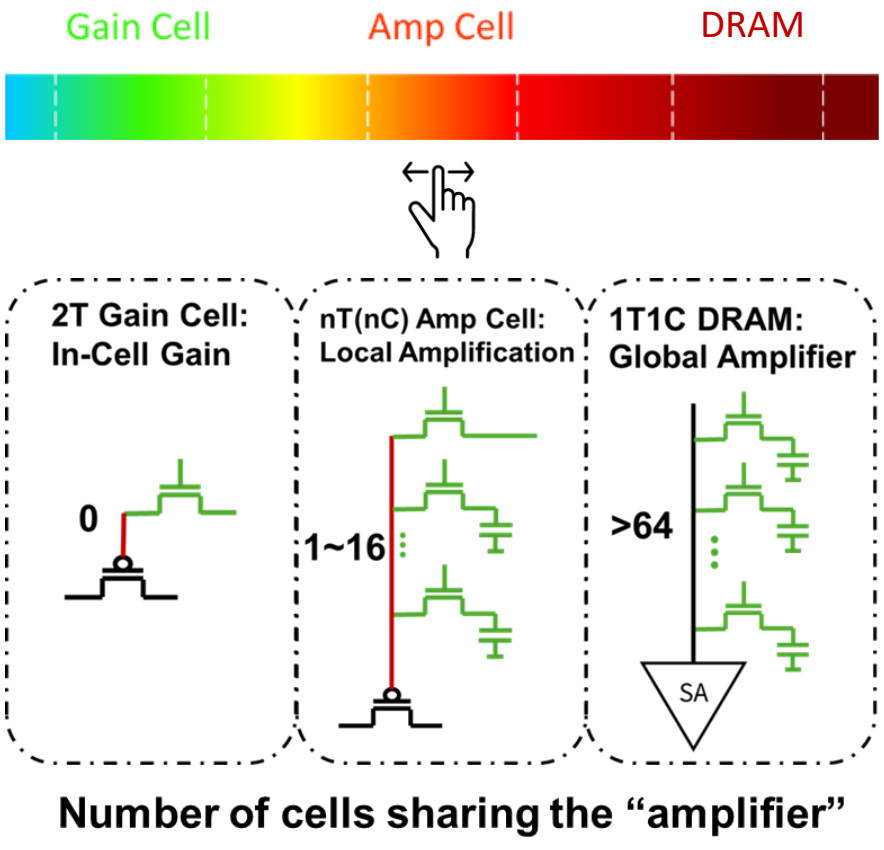
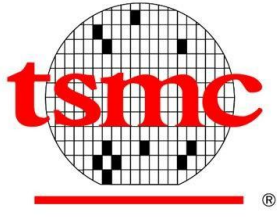
Continuum from 2T Gain Cell to 1T1C DRAM



Acknowledgments


Semiconductor Research Corporation

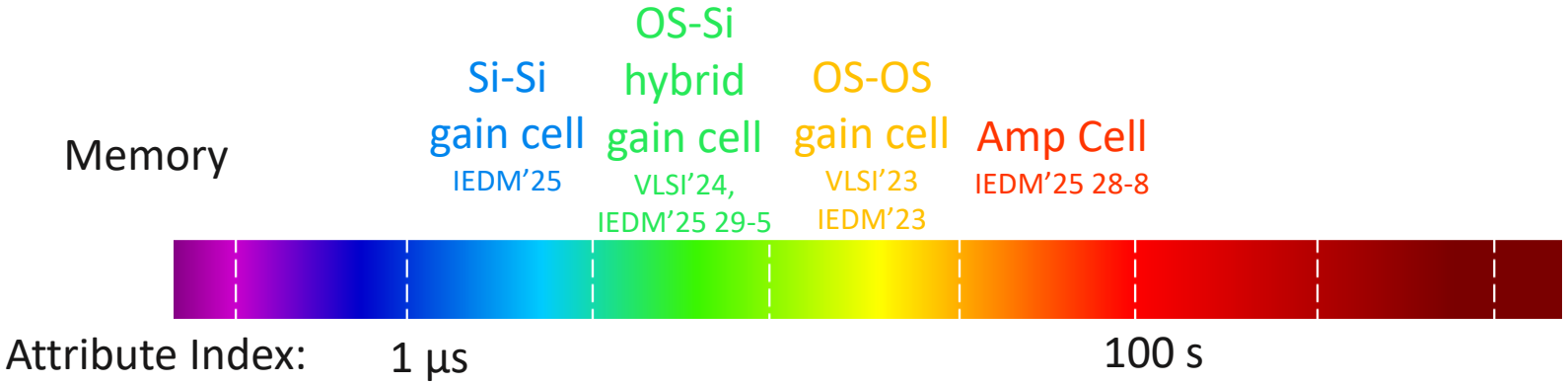


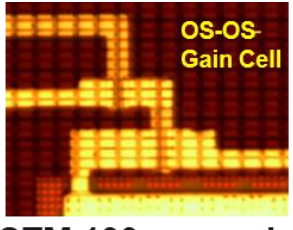
DAM
Stanford Differentiated Access Memories Project

Stanford University

Stanford | NMTRI
NON-VOLATILE MEMORY TECHNOLOGY RESEARCH INITIATIVE

BRIDGE
Blended Retention-Indexed Diverse Gain cEll





STM 130-nm node

TSMC 40-nm node