

Water Bottle Memory

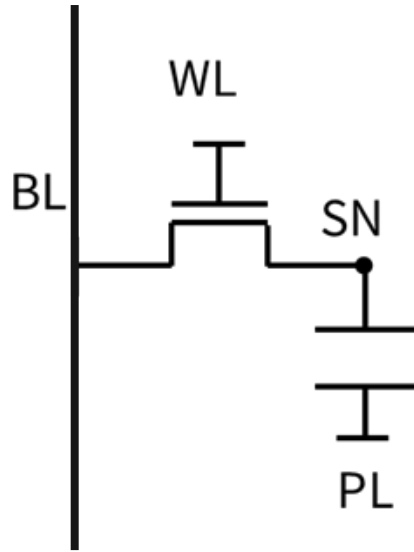


Has water – state “1”
No water – state “0”

How can you tell if there is
water or not?

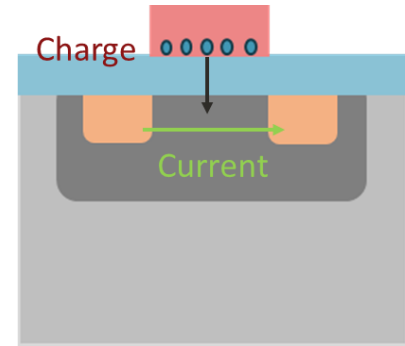
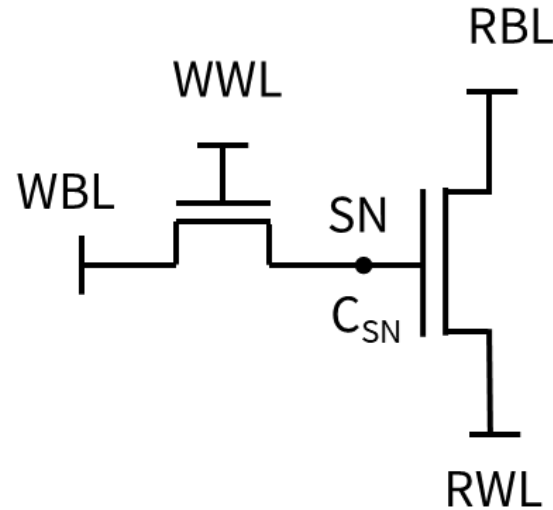
Water Bottle Memory

1T1C DRAM



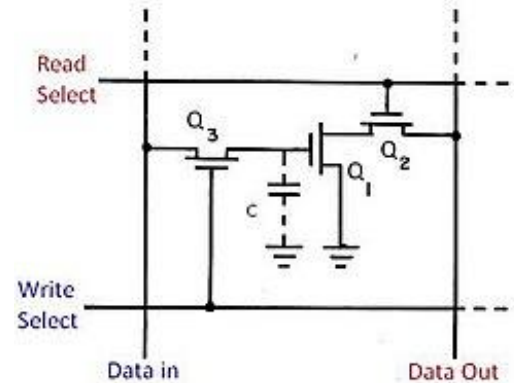
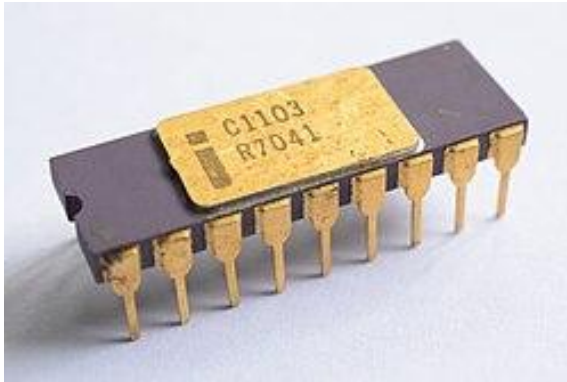
Pour out water to BL tank

2T Gain Cell



Measuring the weight of water

Intel 1103: First Commercial DRAM IC (1970)



Oxide Semiconductor

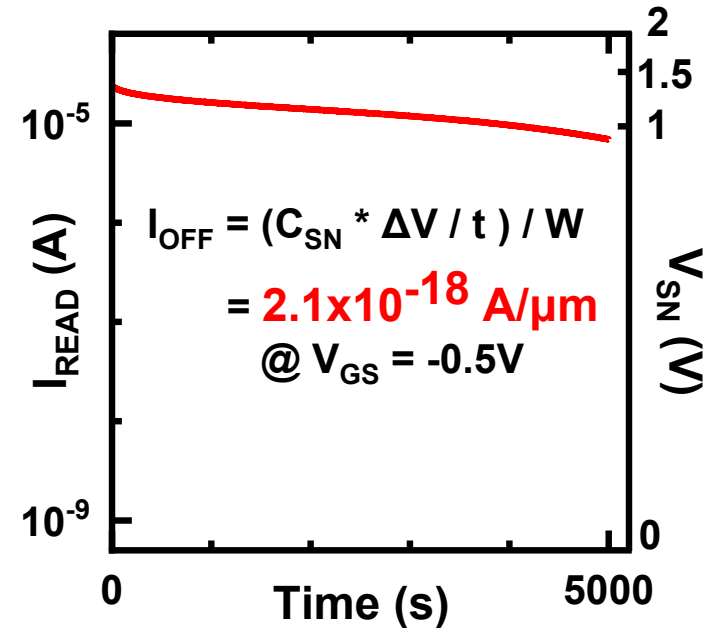
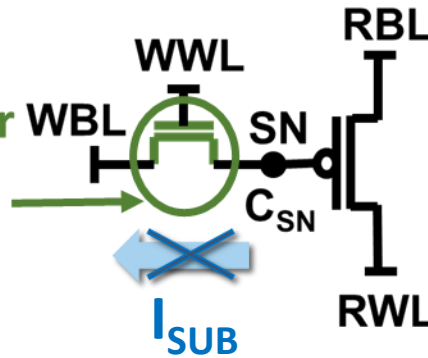
wide bandgap → low leakage → long retention

Oxide Semiconductor
(IGZO, ITO, IWO...)

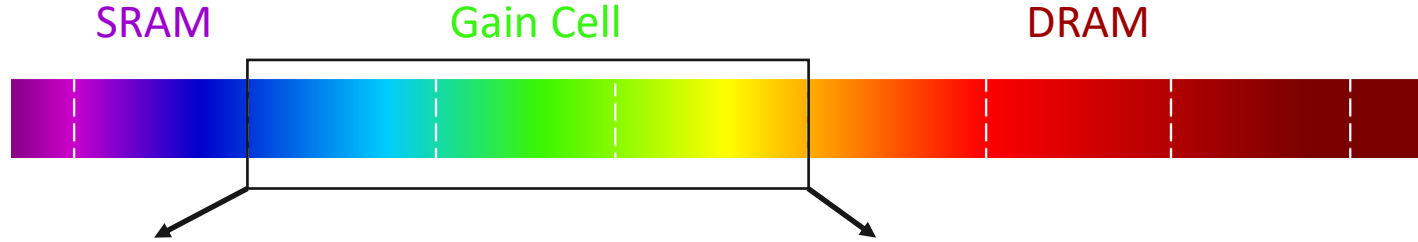
IGZO: Indium Gallium Zinc Oxide

ITO: Indium Tin Oxide

IWO: Indium Tungsten Oxide

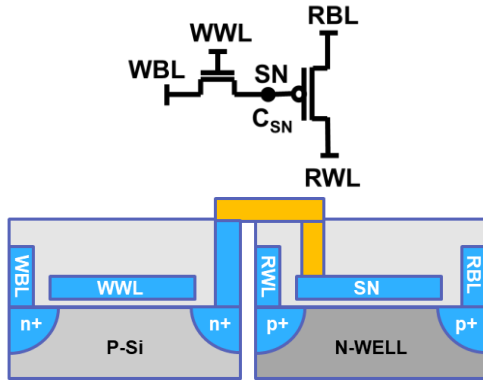


Gain Cell: SRAM-like pseudo-DRAM



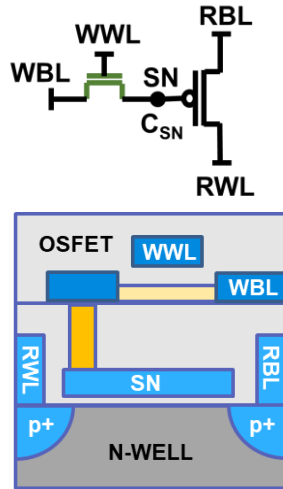
Si-Si gain cell

IEDM'25 28-8 (S. Liu)



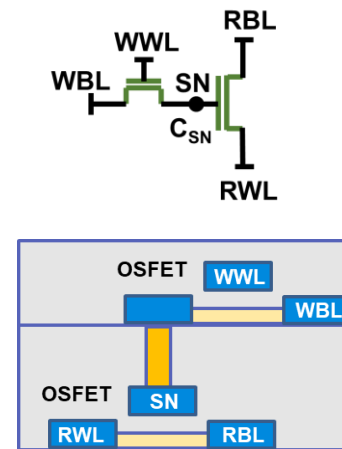
OS-Si hybrid gain cell

VLSI'24, IEDM'25 29-5 (S. Liu)



OS-OS gain cell

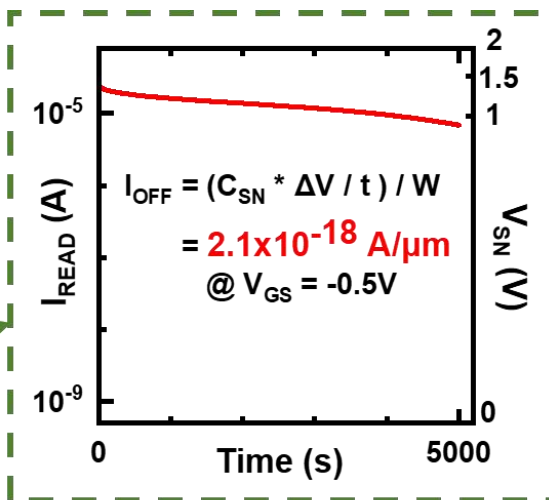
VLSI'23, IEDM'23 (S. Liu)



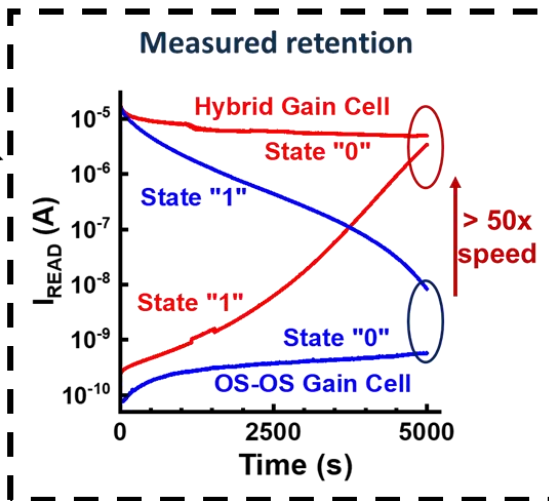
The diagram illustrates the structure and electrical circuit of a 3D NAND device. On the left, a schematic circuit shows a word line (WBL) connected to a transistor gate. The transistor's source is connected to a sense node (SN) and a coupling node (C_{SN}), while its drain is connected to a word line (WWL). The sense node (SN) is connected to a bit line (RBL) and a read word line (RWL). On the right, a 3D perspective view shows the physical structure of the device, including the word lines (WBL, WWL), bit lines (RBL, RWL), and the storage nodes (G, D, OS, S) arranged in a 3D stack. The structure is shown on a substrate with a light blue layer and a grey layer.

- ✓ Low leakage current

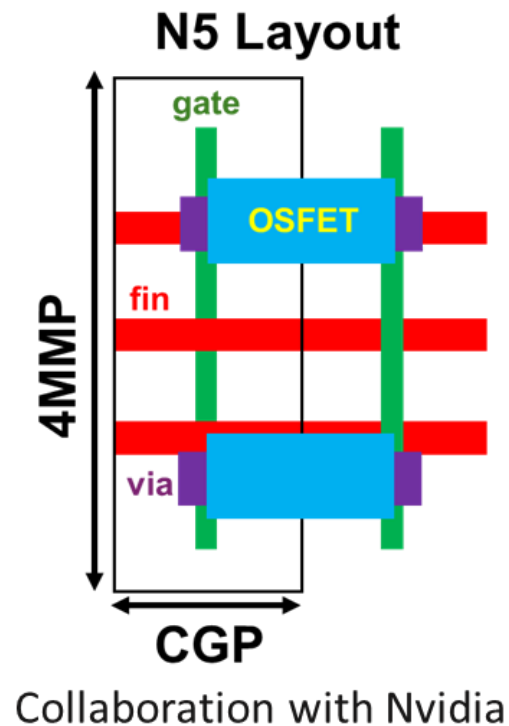
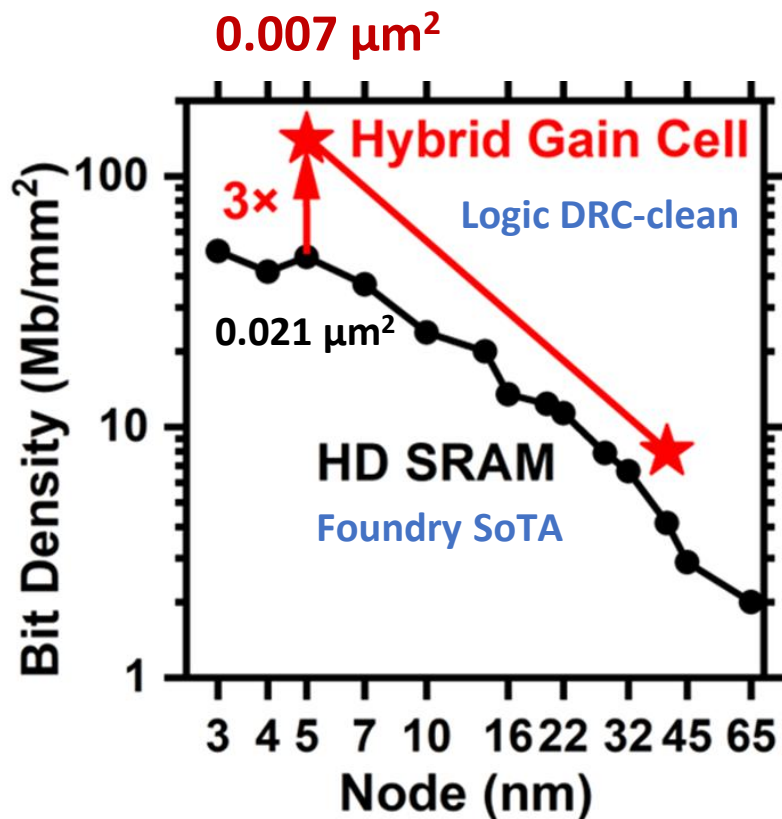
- ✓ **Logic compatible**



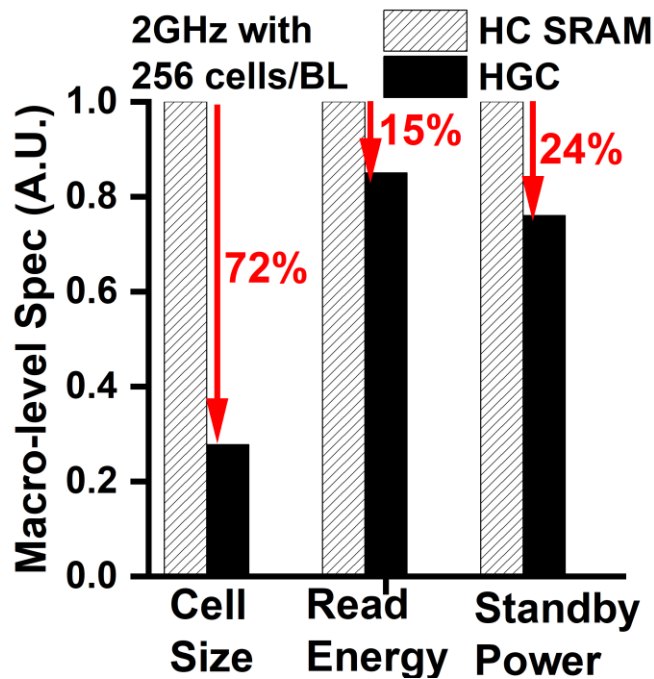
- ✓ **High Mobility (Si)**
- ✓ **Coupling Offset (p-type)**
- ✓ **State Mapping (p-type)**
- ✓ **Bias Reliability (Si)**



Hybrid Gain Cell Array Density 3× of HD SRAM

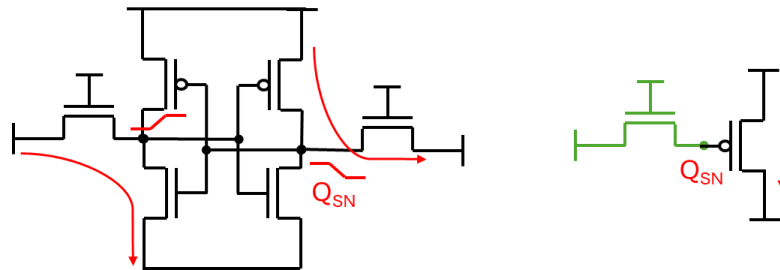


Hybrid Gain Cell Macro Lower Energy than SRAM



Collaboration with Nvidia

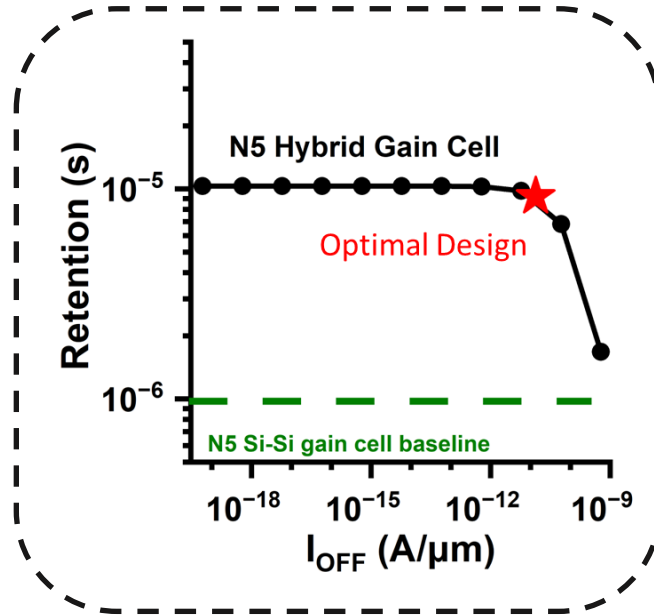
Lower Read Energy than SRAM



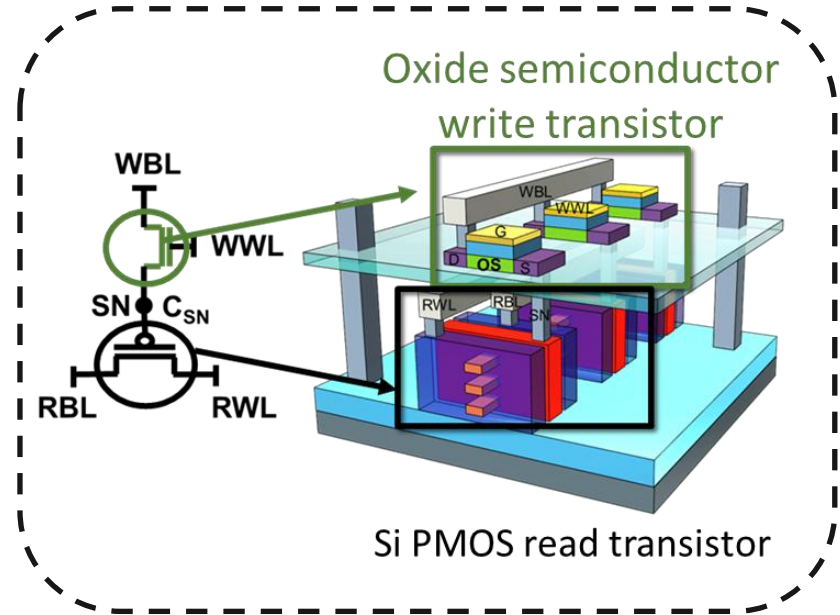
HC SRAM: high-current SRAM
HGC: hybrid gain cell (OS-Si)

Limitation of Hybrid Gain Cell

Retention limited by gate leakage of Si read transistor

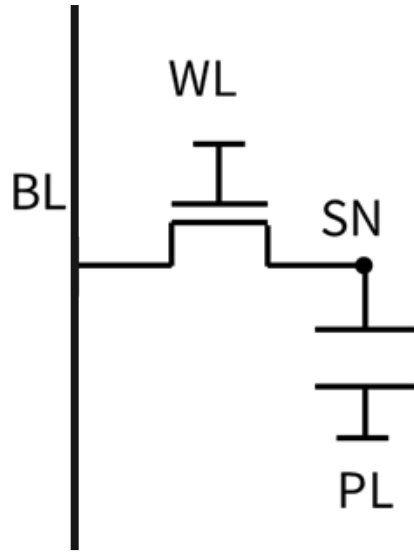


Not 3D-scalable



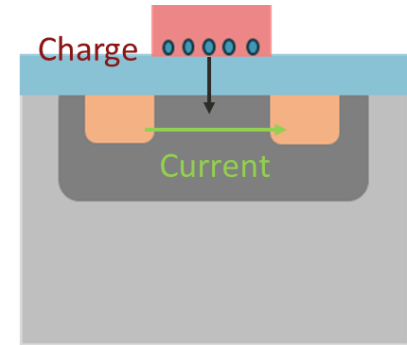
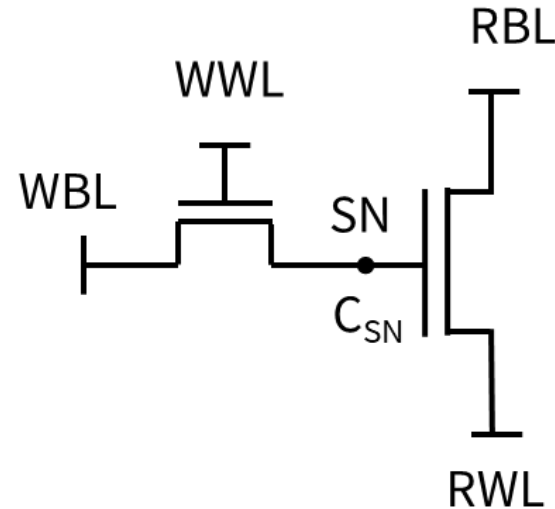
Water Bottle Memory

1T1C DRAM



Pour out water to BL tank

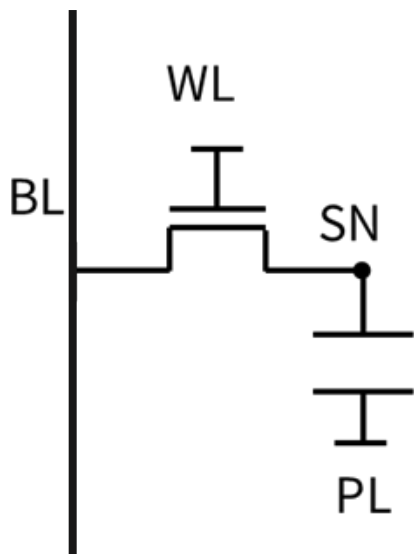
2T Gain Cell



Measuring the weight of water

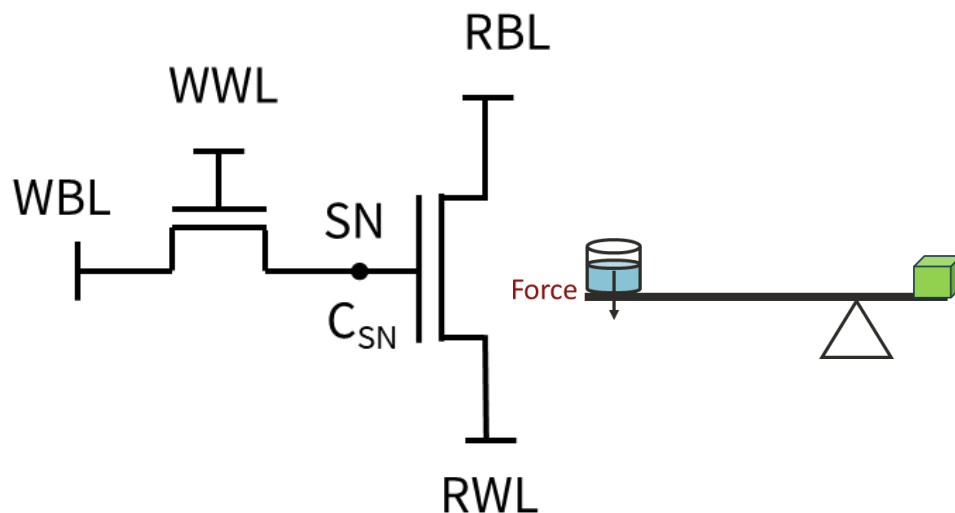
Water Cup Memory (On-chip Small Capacitor)

1T1C eDRAM



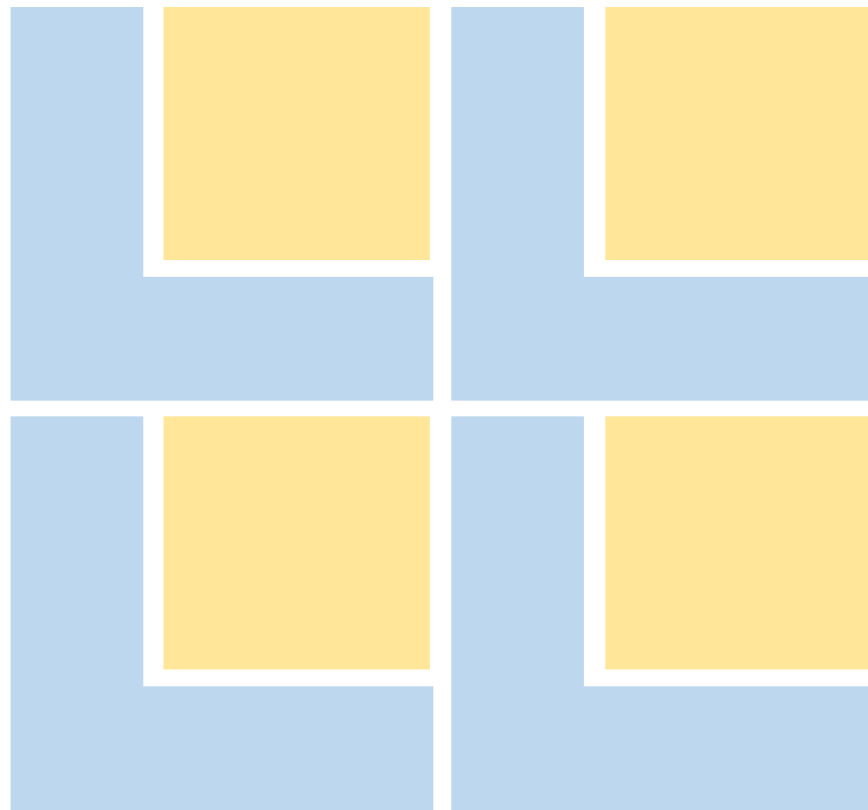
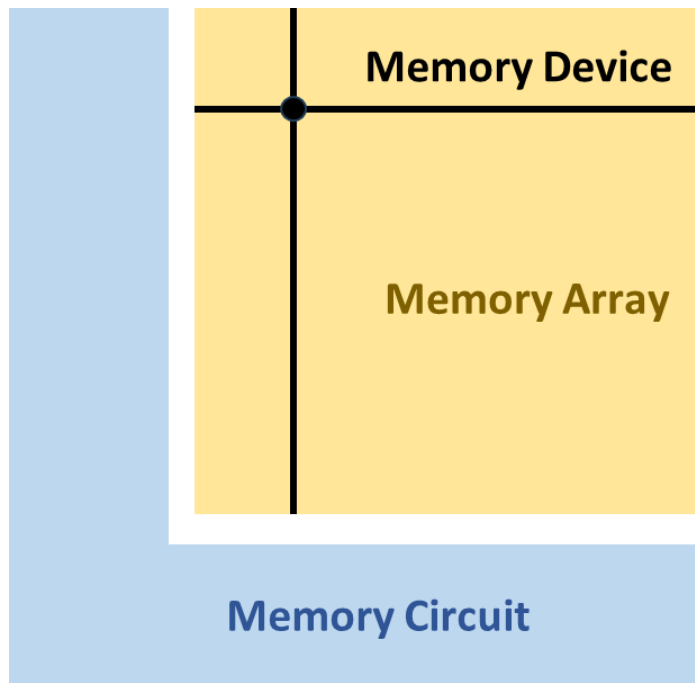
Pour out water to BL tank
-> Smaller tank (shorter BL)

2T Gain Cell

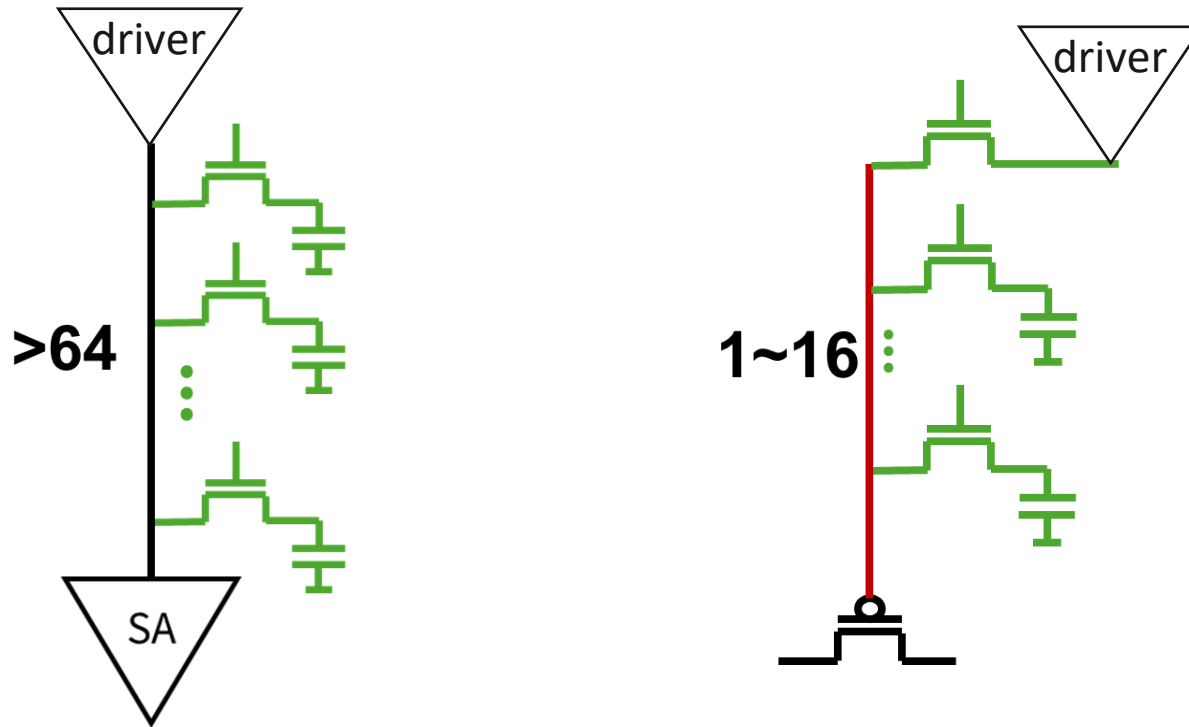


Measuring the weight of water
-> Increase the amplification (Si higher gain)

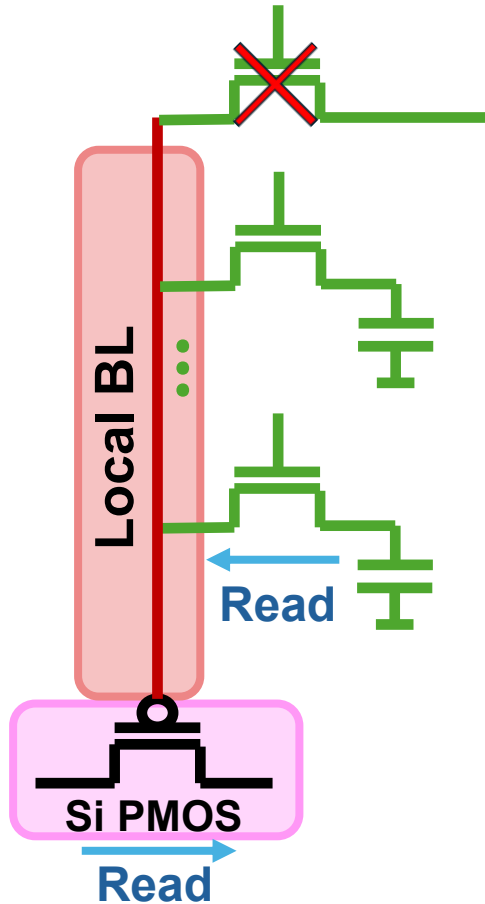
Small Granularity: Lower Area Efficiency



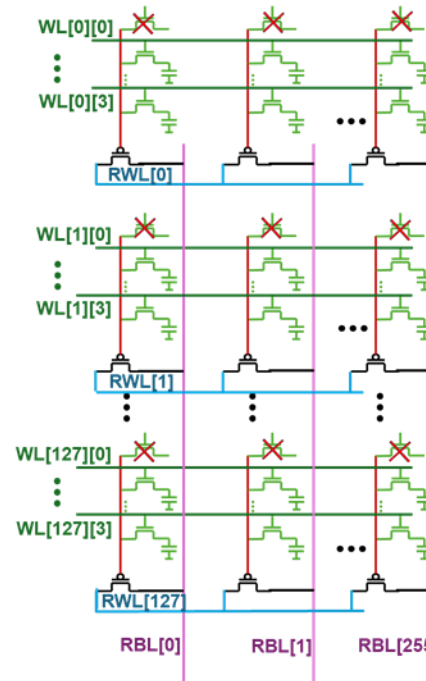
Amp Cell: Area Efficient eDRAM



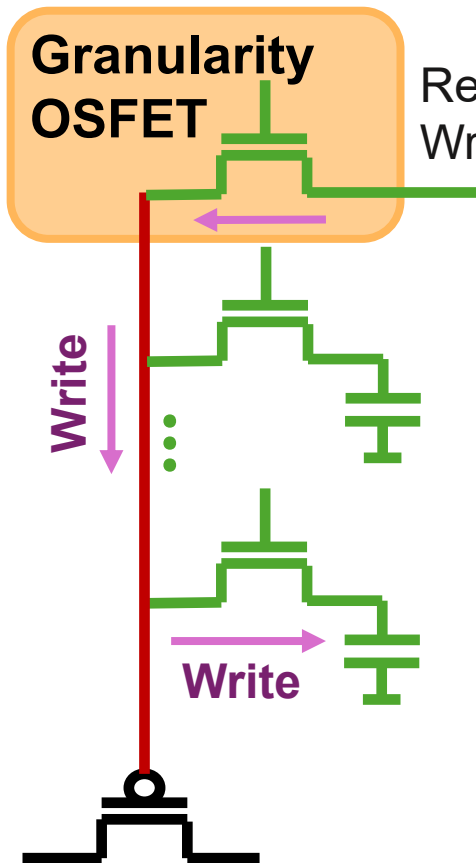
Local Amplification Read



Local Charge Share (4 cells/LBL) +
Read Amplification (128 cells/RBL)

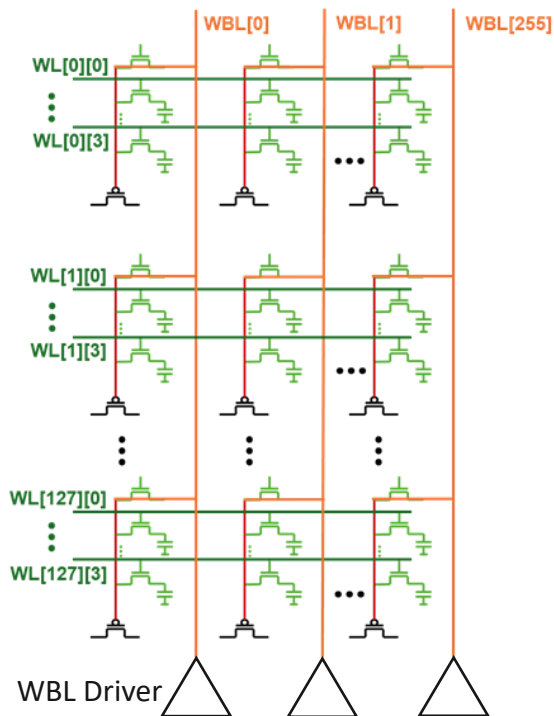


Global Write



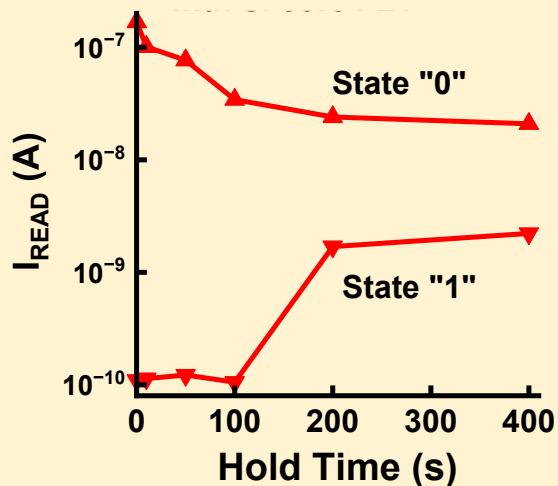
Read: Small Granularity Optimized for Speed
Write: Large Granularity Optimized for Area Efficiency

512 cells/WBL sharing one driver

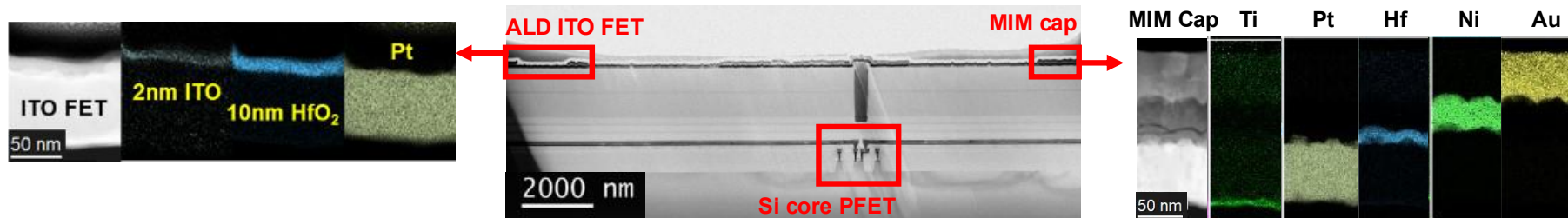
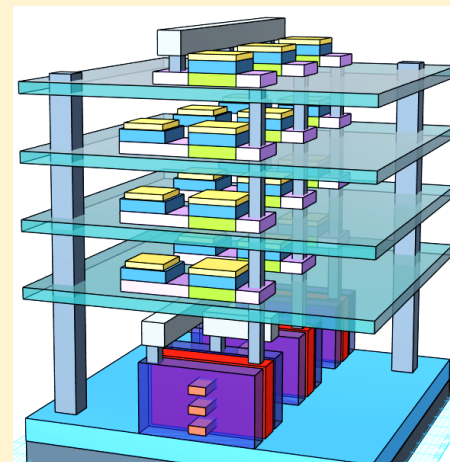


Amp Cell on N40 CMOS+X Chip

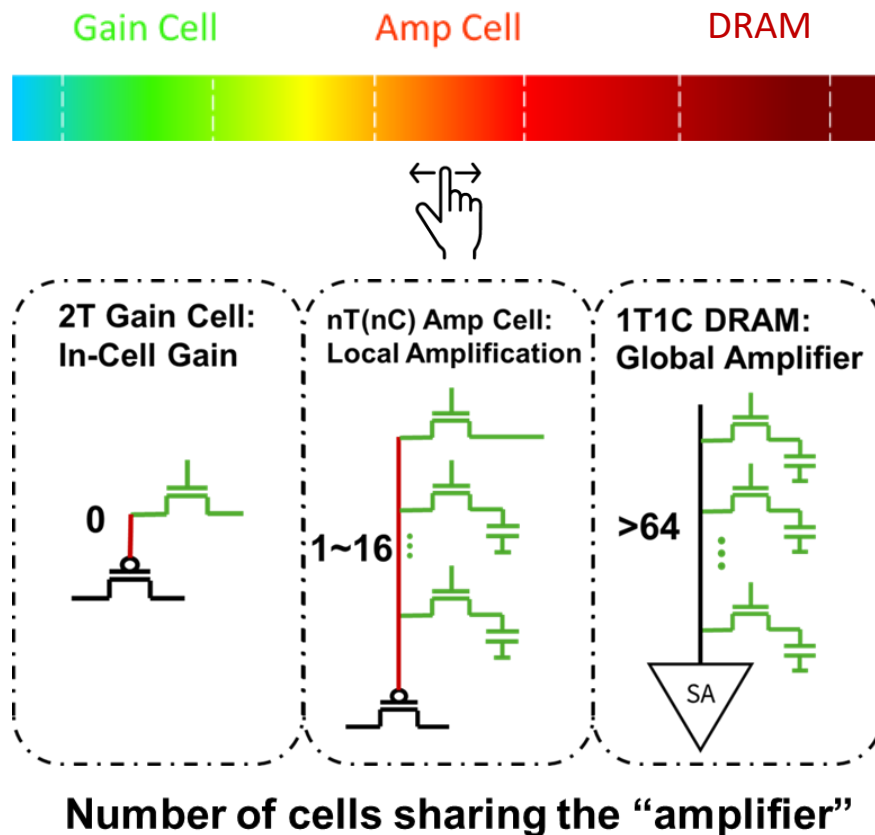
Retention > 5× with same Si core transistor



3D-scalable and logic-compatible



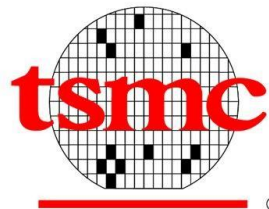
Continuum from 2T Gain Cell to 1T1C DRAM



Acknowledgments



Semiconductor
Research
Corporation



DAM

Stanford Differentiated Access Memories Project

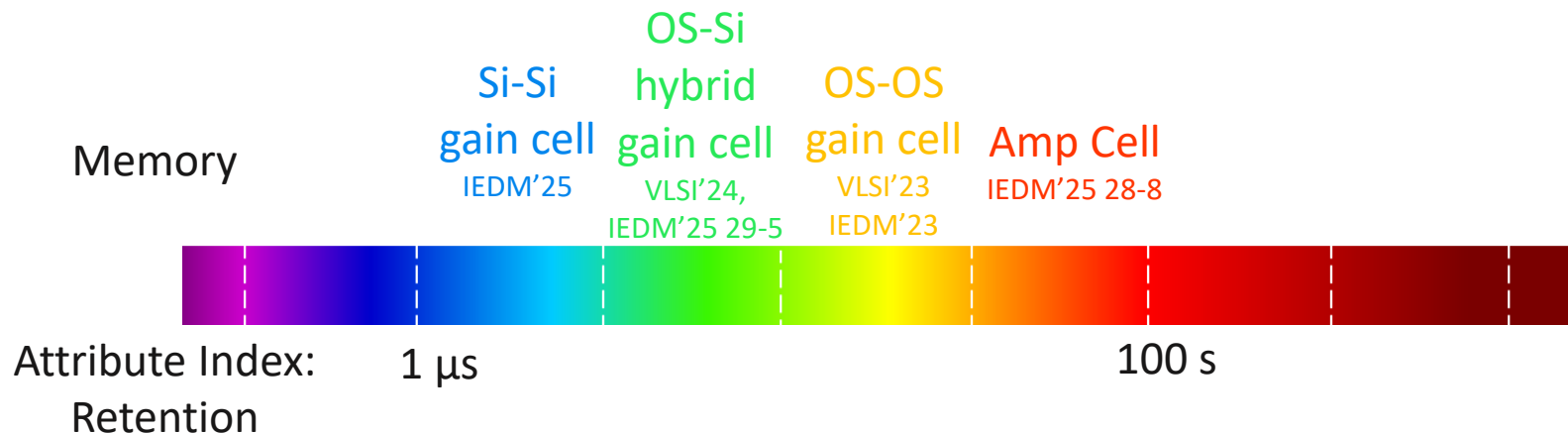


Stanford University

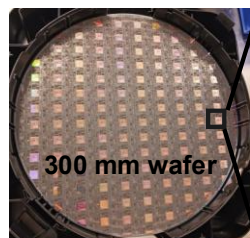
Stanford | NMTRI
NON-VOLATILE MEMORY TECHNOLOGY RESEARCH INITIATIVE

BRIDGE

Blended Retention-Indexed Diverse Gain cEll



STM 130-nm node



TSMC 40-nm node

