Ferroelectrics: Past, Present, and Future

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Willard R. & Inez Kerr Bell Professor, Stanford University

World of Memories

- Incumbents: SRAM, DRAM, Flash
- In products: MRAM, RRAM
- In development in companies and academia:
  - $4F^2$ DRAM and 3D DRAM (horizontal capacitors)
  - Oxide semiconductors for DRAM (1T1C) and gain cell memory (2T,3T,OS-OS,OS-Si, amp cell)
  - Ferroelectrics (1T1C, 1T FeFET)
  - Selector-only-memory (SOM)
- Companies gave up on:
  - Phase change memory
- In academic research: various unproven stuff
  - 2D materials RRAM
  - SOT MRAM
  - Skyrmions

A Short History

Strong increase of number of applications

First Qimonda 65 nm FeFET

FE Tunnel Junctions

DRAM like FeFET

Logic in Memory

FE Cap FRAM

NCFET

2007 2008 2009 2011 2012 2016 2017 2018 2020

Qimonda: FE properties found

First publication

First GF 28 nm FeFET

NV DRAM

Neg. Cap

Piezo/Pyro Devices

Synaptic devices

U. Schroeder (namlab), “Ferroelectric Hafnium Oxide: from Memory to Emerging Applications,” Symp. VLSI Short Course, 2020.

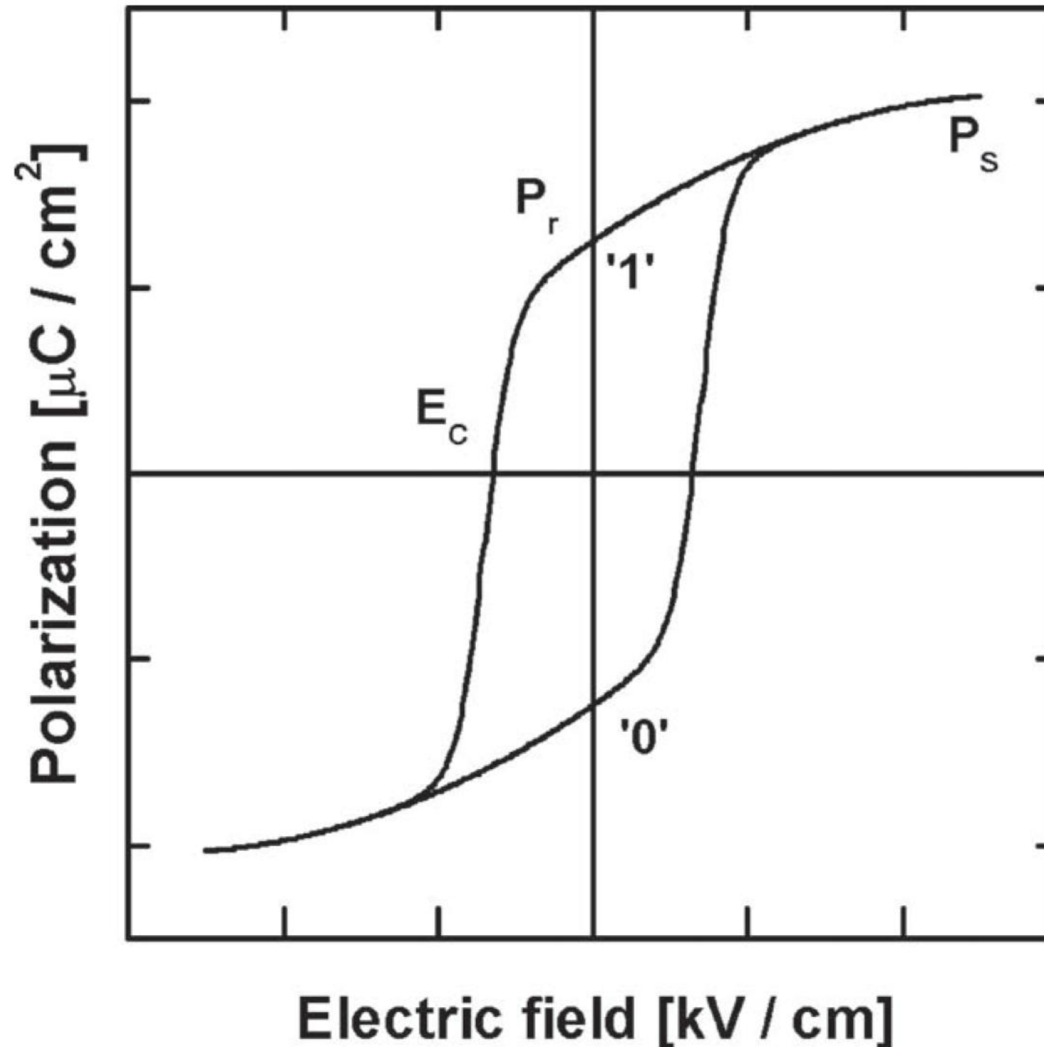
Experts on Ferroelectrics

- U. Schroeder (namlab, Germany), FMC (fabless)
- Suman Datta (Georgia Tech)→ Kai Ni (Notre Dame),
- Shimeng Yu (Georgia Tech)
- Sayeef Salahuddin (Berkeley)→Asif Khan (GaTech)
- Paul McIntyre (Stanford)
- IMEC, Peking U, Chinese Academy of Sciences

State-of-the-Art

- 1T1C FeRAM – Micron, SONY, IMEC, LETI
  - Key questions:
    - Endurance cycles (1E11)
    - On-chip (>10s ns) or stand-alone (bit density < DRAM)?
- 1T FeFET – planar → 3D, Si channel → oxide channel
  - Key questions:
    - High-capacity (many layers) not yet demonstrated
    - Ferro + oxide channel: many materials questions still
    - Stability, 100 ns write, 10’s us erase, read-delay-after-write,

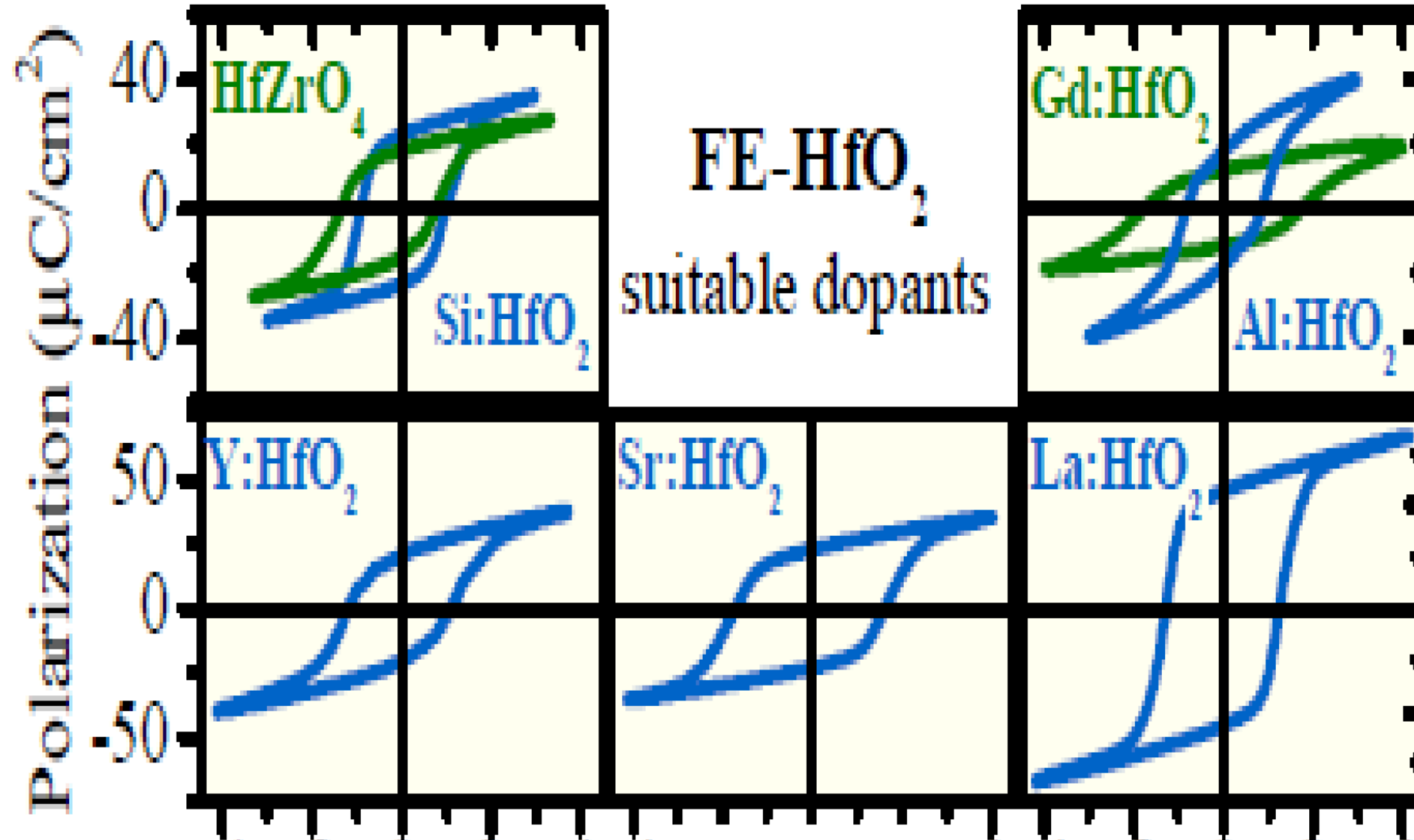
Ferroelectric Polarization



- 1 μC/cm^2 = 1.9 × 10^{13} q/cm^2
- This is quite a large charge density.
- Typical charge density under Si FET gate in on-state is about mid-10^{13} q/cm^2

J. Hoffman… T.P. Ma, Ferroelectric Field Effect Transistors for Memory Applications," Adv. Mater. P. 2957, 2010.

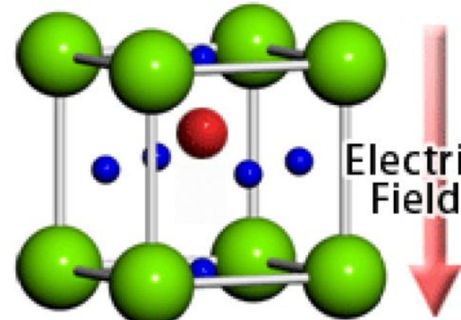
Doped HfO_2



T.P. Ma, "FEDRAM: A capacitor-less DRAM based on ferroelectric-gated FET," IEEE IMW, 2014

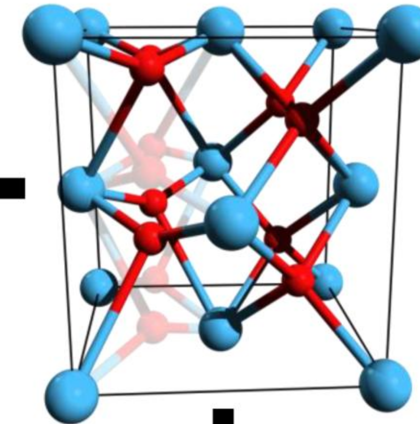
PZT (Lead Zirconium Titanate) vs Ferroelectric HfO2

Perovskite Crystal Structure



Fujitsu, 2019

Orthorhombic Crystal Structure



Large P_r
20 – 30 $\mu C/cm^2$

High Curie Temp.
(> 300°C)

$\varepsilon_r \approx 300 - 800$

$E_c \approx 30 - 200$ kV/cm

Scaling Limited > 70nm
(dead layer, depol. effects)

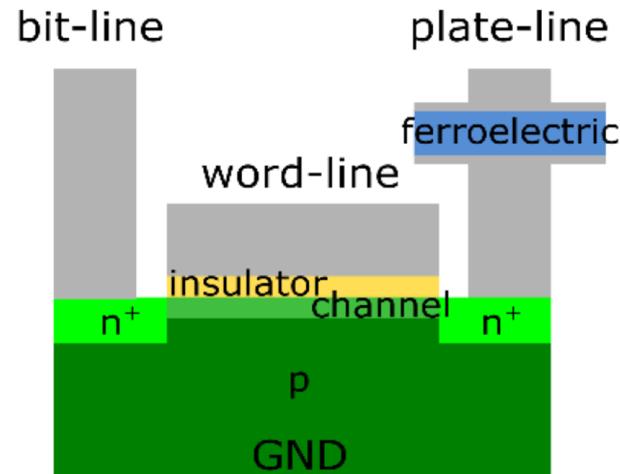
$\varepsilon_r \approx 30 - 40$

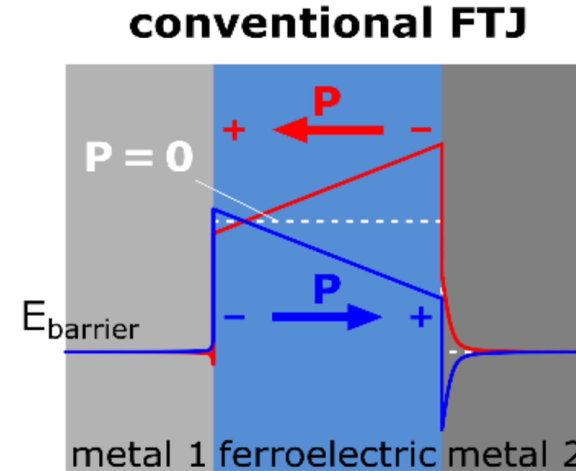
$E_c \approx 1$ MV/cm

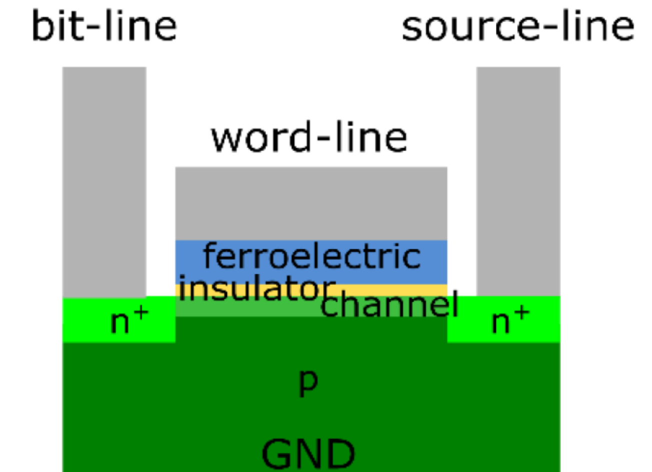
Scaling to < 5nm

U. Schroeder (namlab), "Ferroelectric Hafnium Oxide: from Memory to Emerging Applications," Symp. VLSI Short Course, 2020.

Ferroelectric Memories

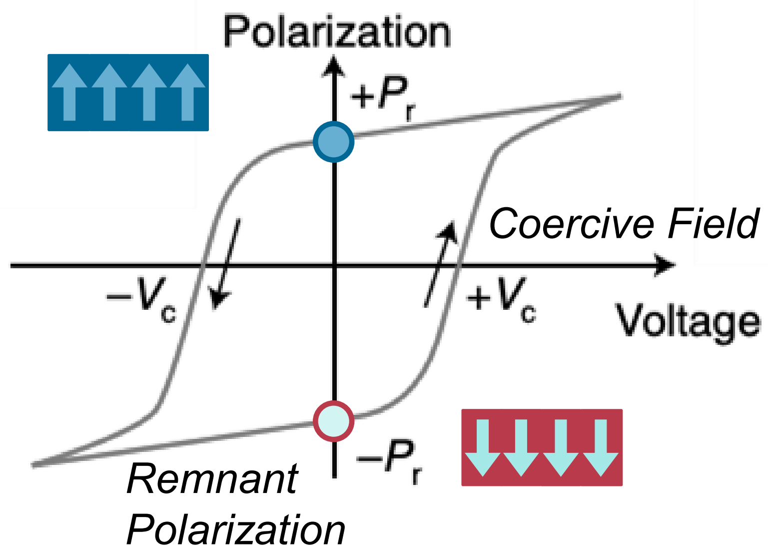






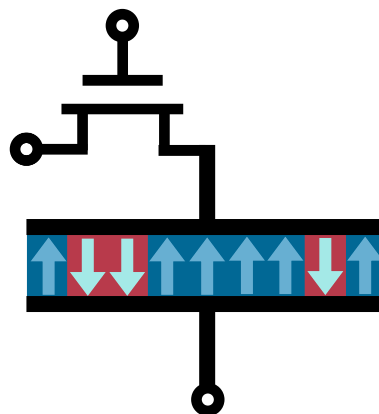
U. Schroeder (namlab), "Ferroelectric Hafnium Oxide: from Memory to Emerging Applications," Symp. VLSI Short Course, 2020.

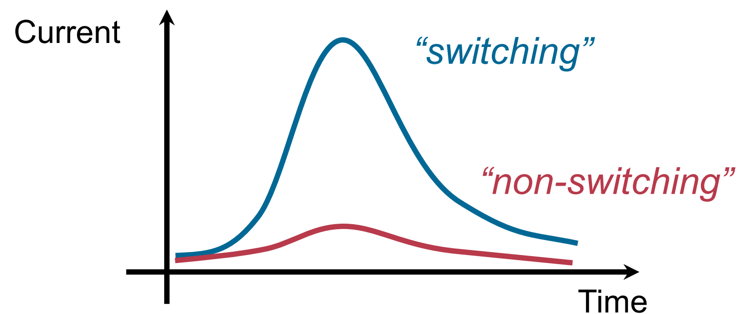
Ferroelectric Memories: Operation Principles



FeRAM (1T1C)

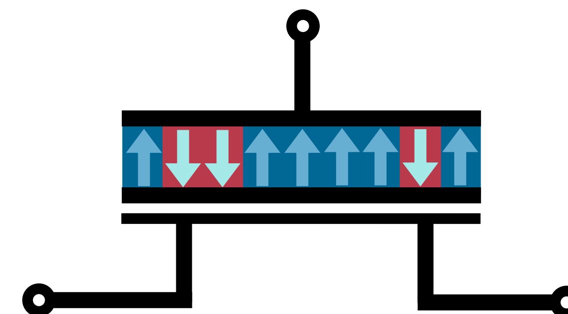
Ferroelectric Random-Access Memory
"DRAM-like"

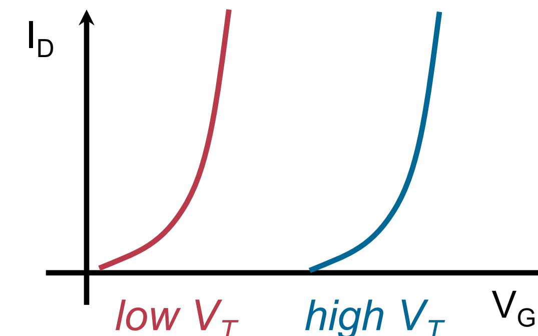




FeFET (1T)

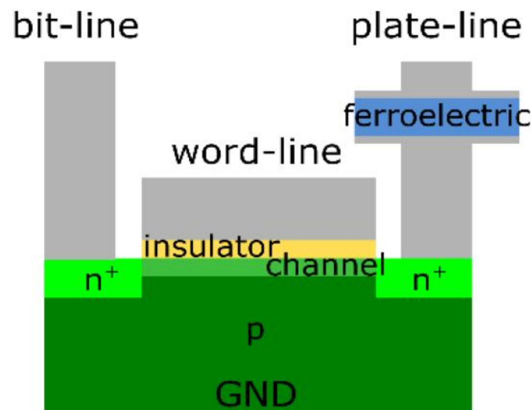
Ferroelectric Field-Effect Transistor
"FLASH-like"

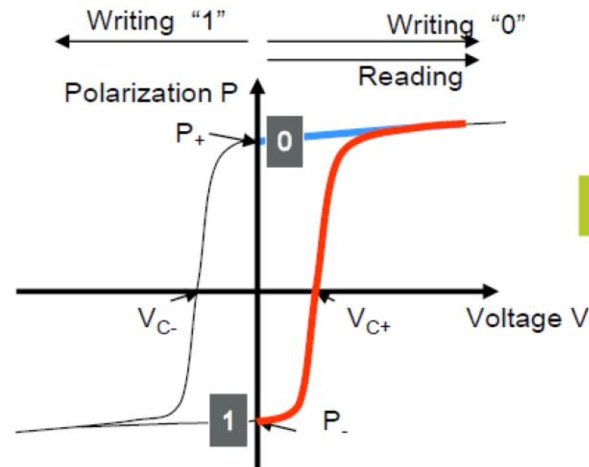


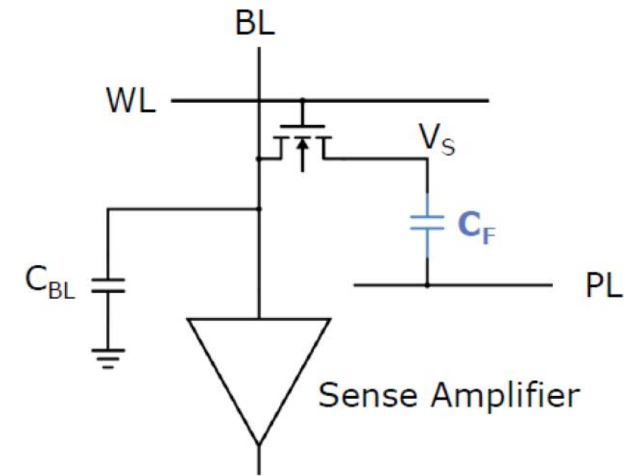


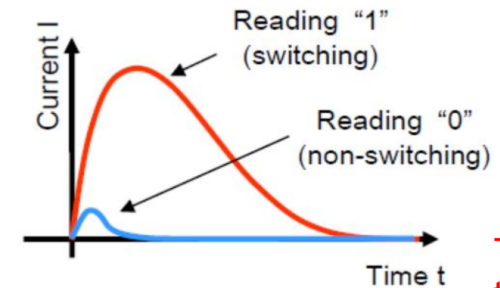
1T1C – Destructive Read

- Memory: polarization state on the MIM (MFM) capacitor
- Read operation destroys the data stored, need to re-write information back
- Every read is a write – very high endurance required.









Total charge that flipped

$$\Delta V_{BL}("0") \approx 0 \qquad \Delta V_{BL}("1") = \frac{2P_r \cdot A}{C_F + C_{BL}}$$

U. Schroeder (namlab), "Ferroelectric Hafnium Oxide: from Memory to Emerging Applications," Symp. VLSI Short Course, 2020.

FeFET Memory

Source
Gate
Drain
buffer 1
ferroelectric
buffer 2
n^+
n^+
p-Si

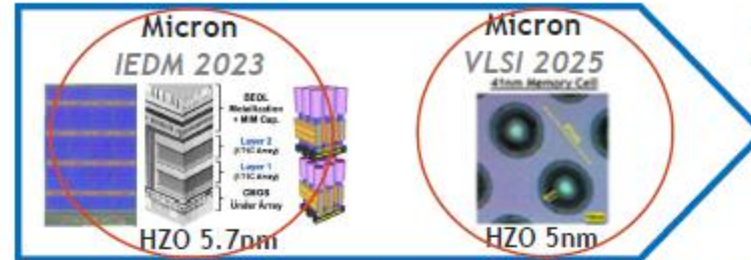
SL(n)
SL(n+1)
WL(m)
2F
WL(m+1)
2F
BL(n)
BL(n+1)

J. Hoffman… T.P. Ma, Ferroelectric Field Effect Transistors for Memory Applications," Adv. Mater. P. 2957, 2010.

1T1C FeRAM

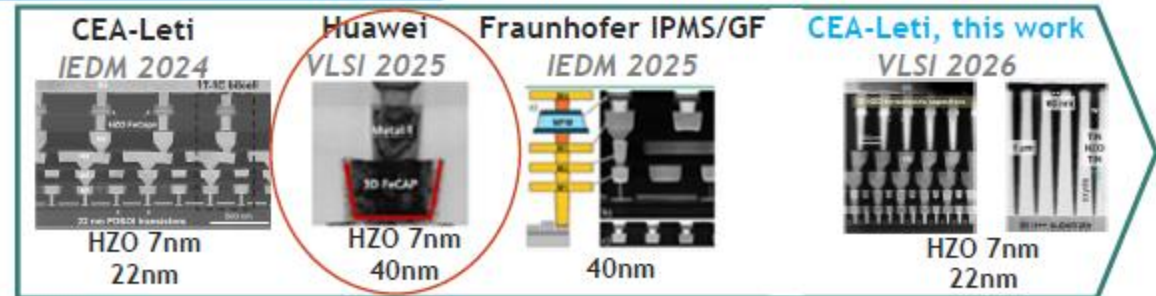
HZO FeRAM arrays: technology achievements

standalone
48nm pitch
300mm



3D FeCap

embedded
22nm node
40nm node
300mm



3D FeCap

3D FeCap
22nm node

embedded
130nm node
200mm

3D FeCap

- So far Embedded 22nm FeRAM arrays reported with 2D FeCaps

T9-4 2026 IEEE VLSI Symposium on Technology and Circuits Slide 9

3D 1T1C FeRAM (32Gb stand alone chip)

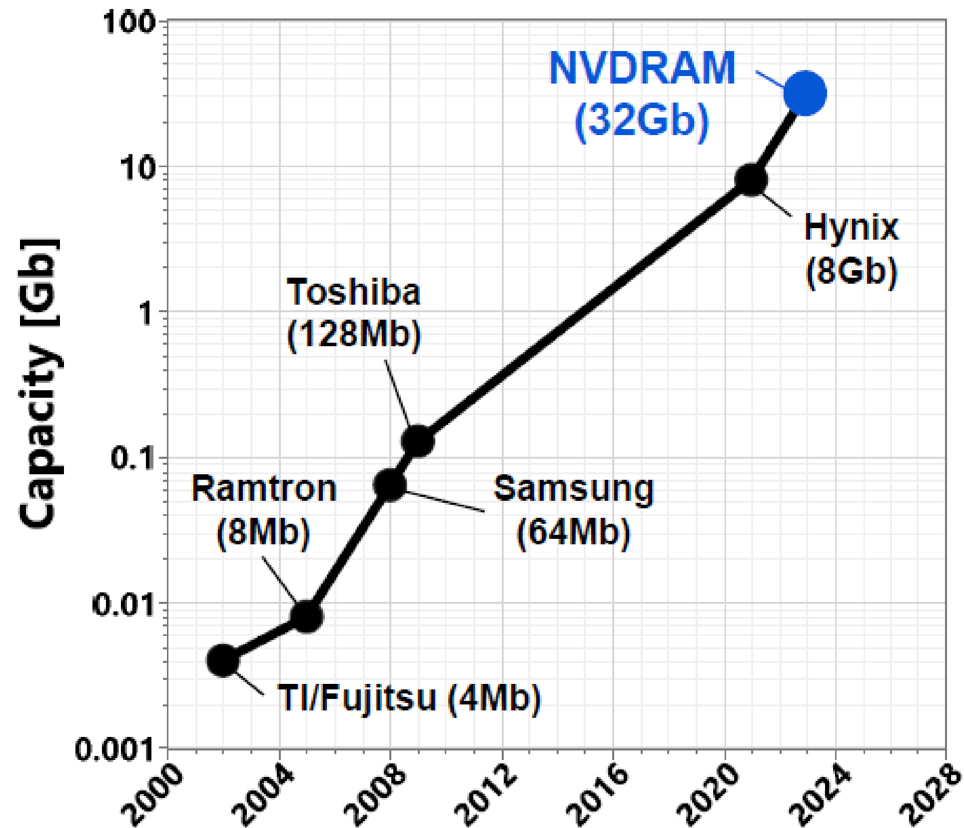


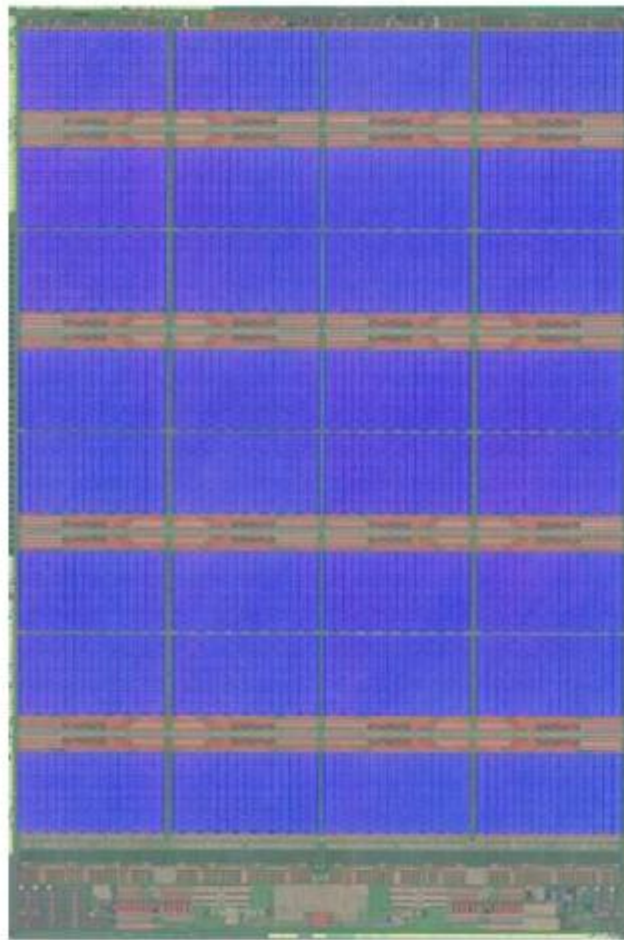
Figure 4. Capacity versus time for ferroelectric memories reported by various companies. NVDRAM uses 1T1C dual-layer memory to achieve 32Gb at 0.45Gb/mm^2 bit density. [3-7]

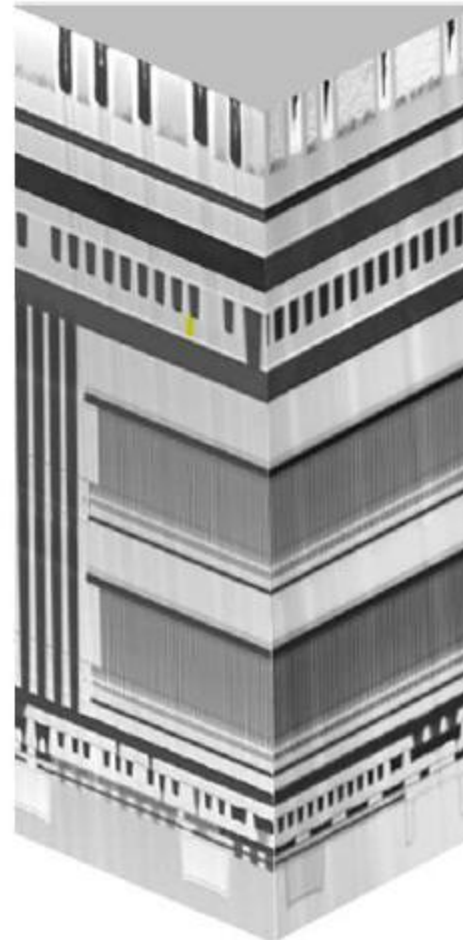
N. Ramaswamy *et al.*, "NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads," paper 15.7, *2023 IEDM*.

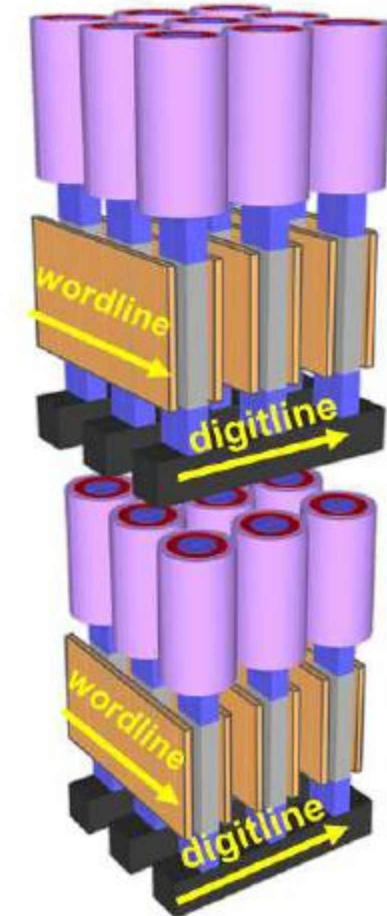
SOTA Bit Density:
Flash: 28.5 Gb/mm²: The Samsung V9 QLC architecture (incorporating around 280 layers) and Samsung's 10th Gen V-NAND (featuring over 400 active layers with hybrid bonding). [1, 2, 3] **29 Gb/mm²:** The Kioxia BiCS10 architecture (featuring 332 active word-line layers) uses CMOS Direct Bonded Array (CBA) technology to maximize integration efficiency. [1, 2, 3]

- **SRAM**: 38 Mb/mm^2 (2 nm)
- **HBM**: 160 Mb/mm^2 (due to TSV)
- **Hybrid gain cell (HGC)**: 150 Mb/mm^2 (5nm node, one layer)
- **DRAM**: 240 – 440 Mb/mm^2 (1a/1b/1c)
- **3D 1T1C FeRAM** 450 Mb/mm^2 (2-layers)

3D 1T1C FeRAM (32Gb stand alone chip)







N. Ramaswamy *et al.*, "NVDRAM: A 32Gb Dual Layer 3D Stacked Non-volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads," paper 15.7, *2023 IEDM*. [Micron]

Vertical Access Transistor and Capacitor

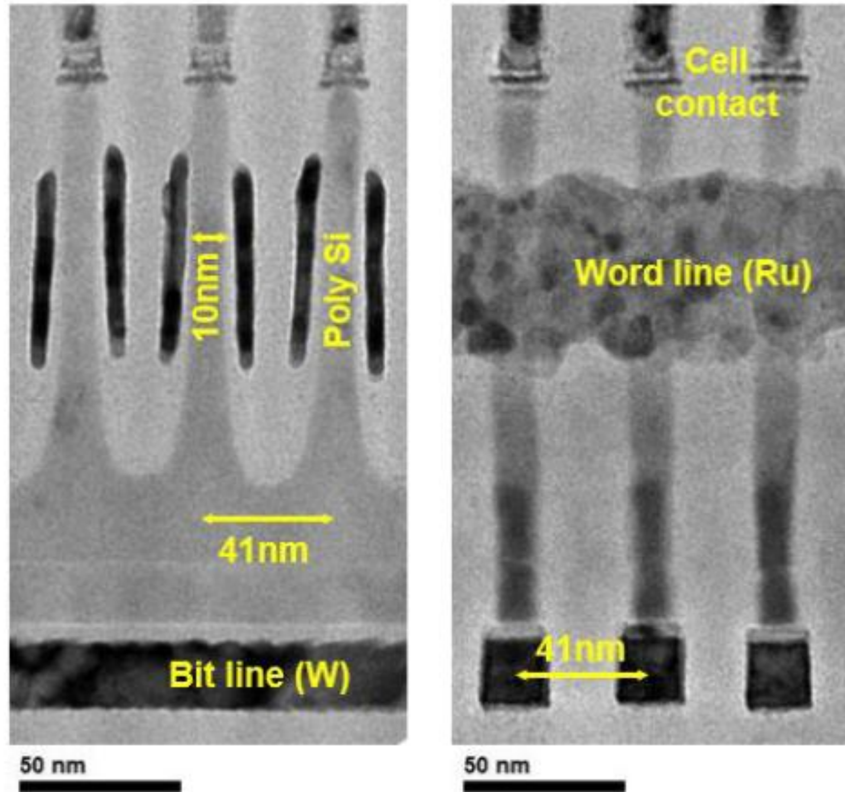


Fig. 1. TEM cross-sections of the Access Device with vertical polycrystalline Silicon channel and Ruthenium dual gate. Pitch is 41nm in both x- and y-direction.

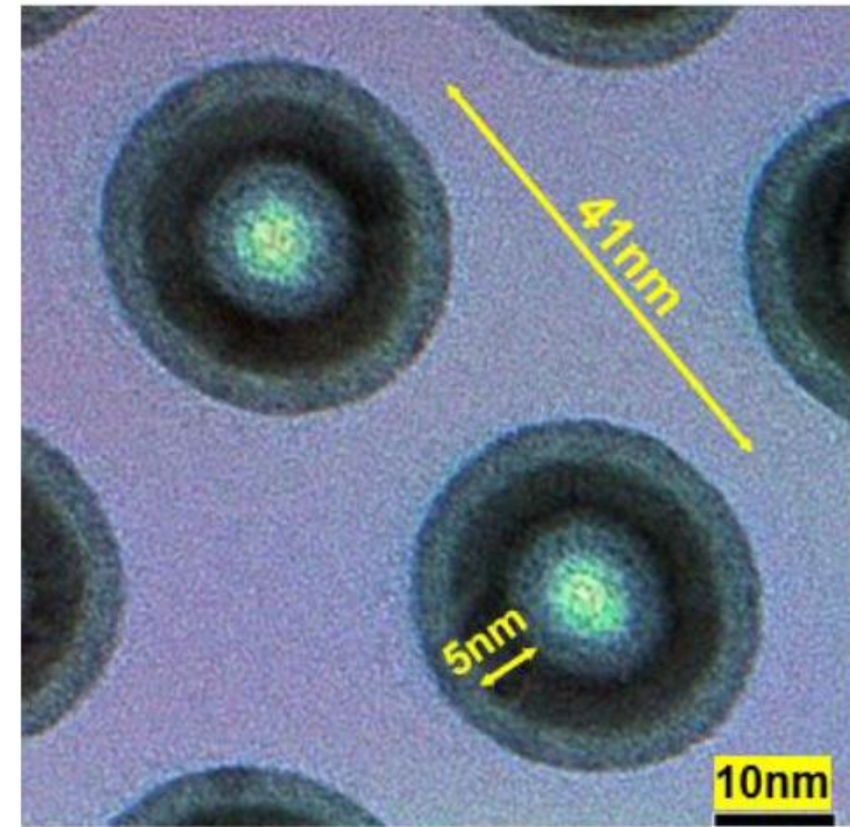


Fig. 5. Planar TEM image of the Memory Cell with TiN based electrodes and $HfZrO_x$ ferroelectric. The ferroelectric thickness is 5nm at 41nm pitch.

A. Calderoni *et al.*, "**Voltage Reduction (1.4V) and Array Scaling (41nm)** of Ferroelectric NVDRAM for Low-Power and High-Density Applications," paper 6-2, *2025 Symp. VLSI.* [Micron]

Advantage over Flash: Voltage

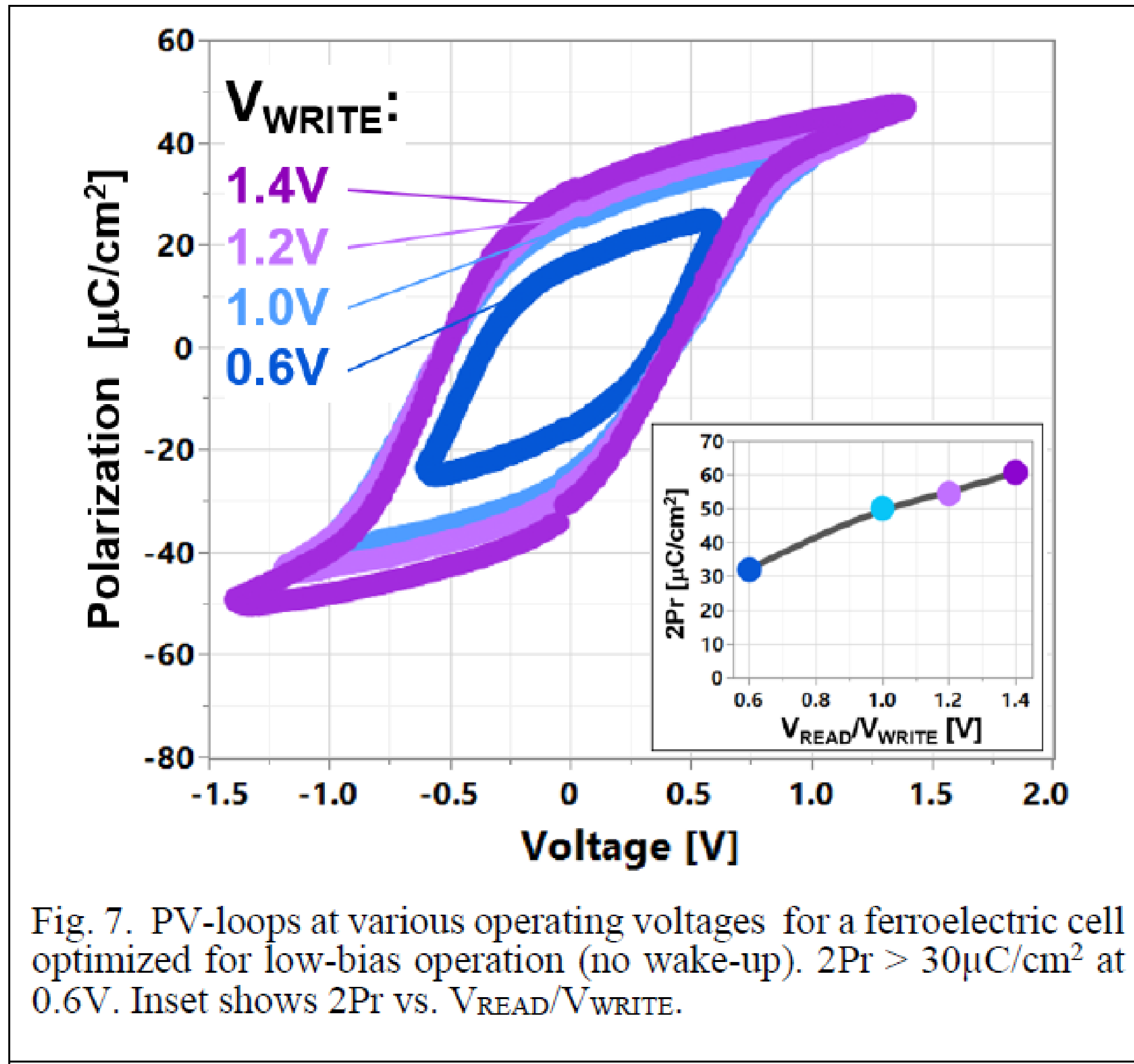


Fig. 7. PV-loops at various operating voltages for a ferroelectric cell optimized for low-bias operation (no wake-up). 2Pr > 30μC/cm² at 0.6V. Inset shows 2Pr vs. V_{READ}/V_{WRITE}.

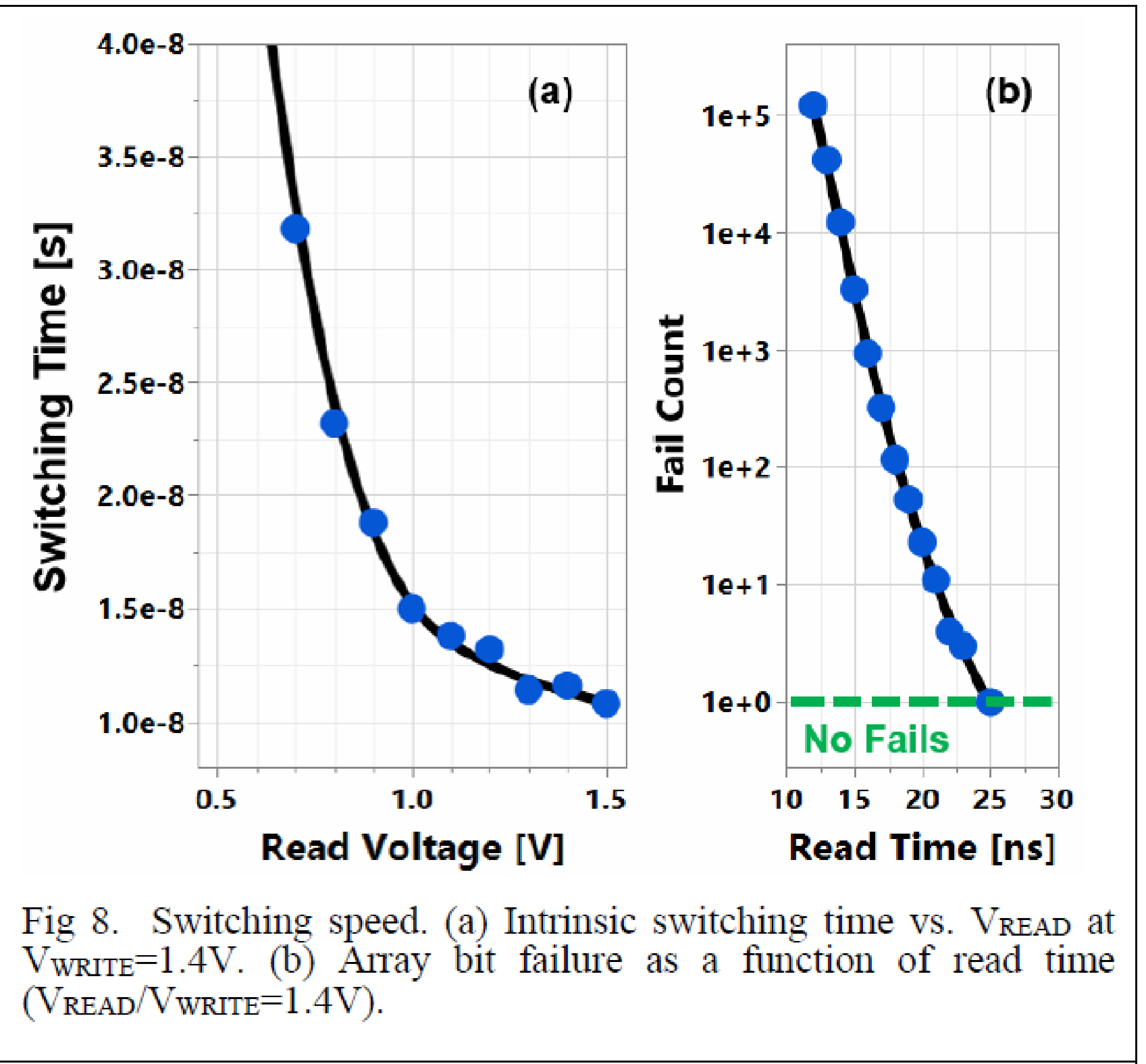


Fig 8. Switching speed. (a) Intrinsic switching time vs. V_{READ} at V_{WRITE}=1.4V. (b) Array bit failure as a function of read time (V_{READ}/V_{WRITE}=1.4V).

A. Calderoni *et al.*, "**Voltage Reduction (1.4V) and Array Scaling (41nm)** of Ferroelectric NVDRAM for Low-Power and High-Density Applications," paper 6-2, *2025 Symp. VLSI.* [Micron]

1.4V, 500 mV Memory Window, 1E10 cycles

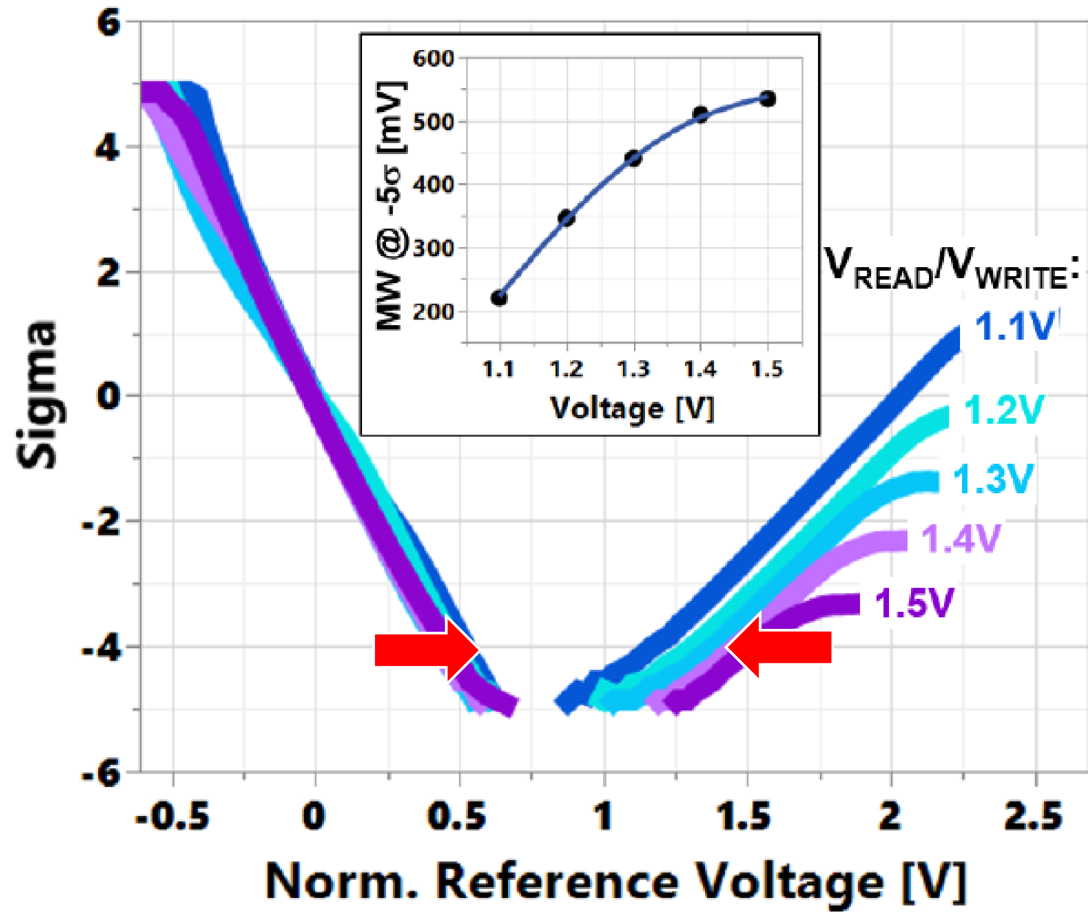


Fig. 9. Array distributions and Memory Window (inset) vs. read/write voltage across the Memory Cell at 35°C.

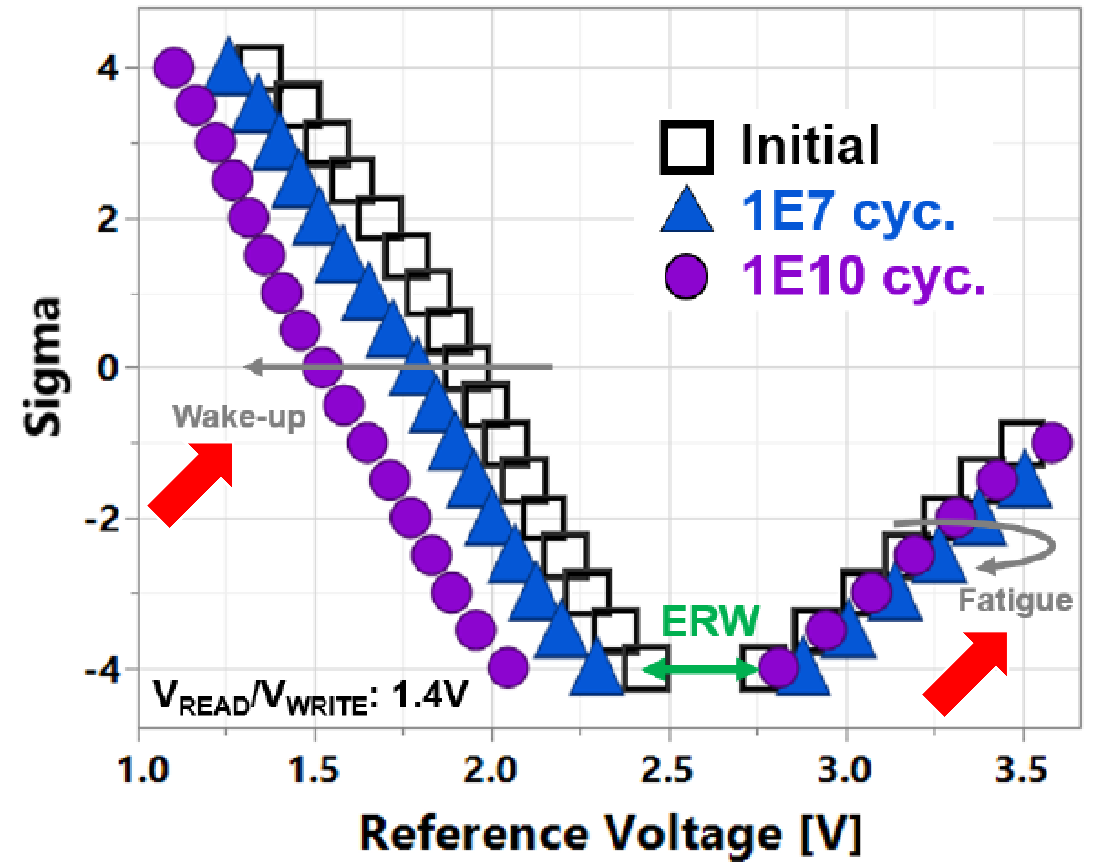


Fig. 10. Endurance characteristics of a 5nm ferroelectric stack operating at 1.4V, 95°C. An Effective Read Window (ERW) greater than 250mV is achieved through 1E10 cycles.

A. Calderoni *et al.*, "**Voltage Reduction (1.4V) and Array Scaling (41nm)** of Ferroelectric NVDRAM for Low-Power and High-Density Applications," paper 6-2, *2025 Symp. VLSI.* [Micron]

1.4V, 500 mV Memory Window, 1E10 cycles

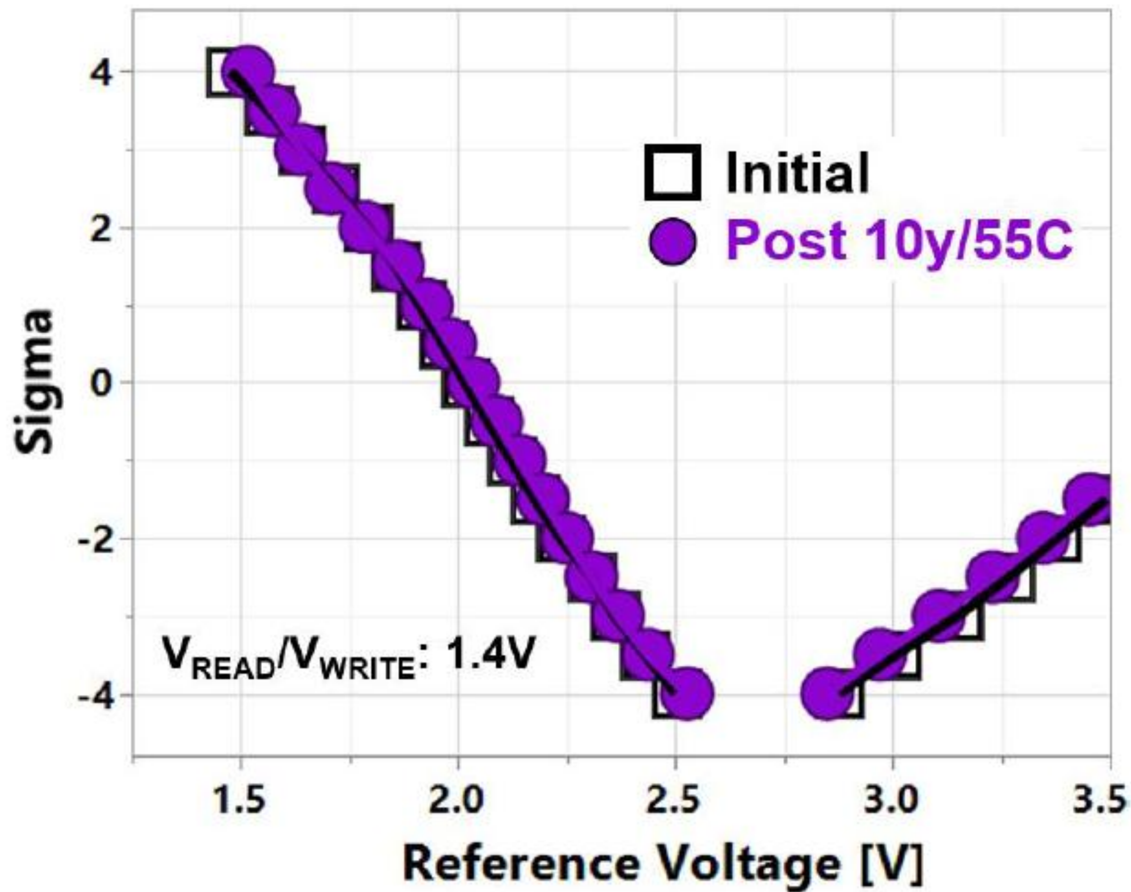


Fig. 11. Retention characteristics of a 5nm ferroelectric stack operating at 1.4V.

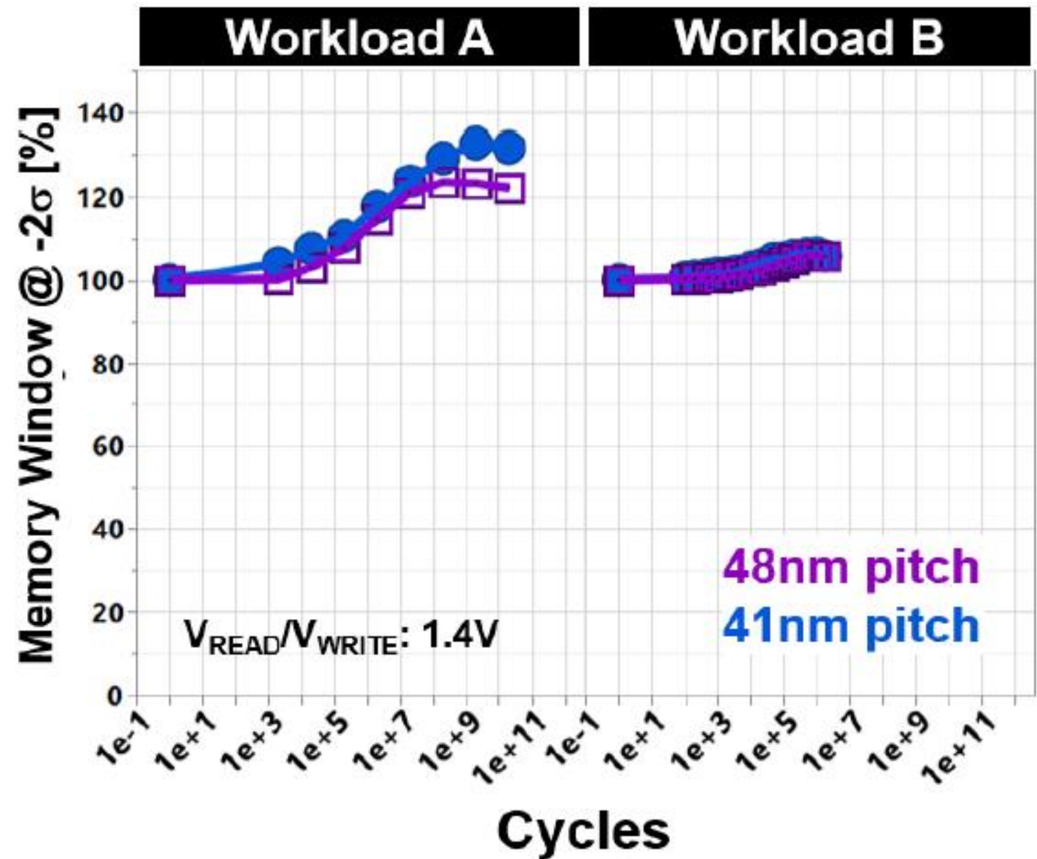
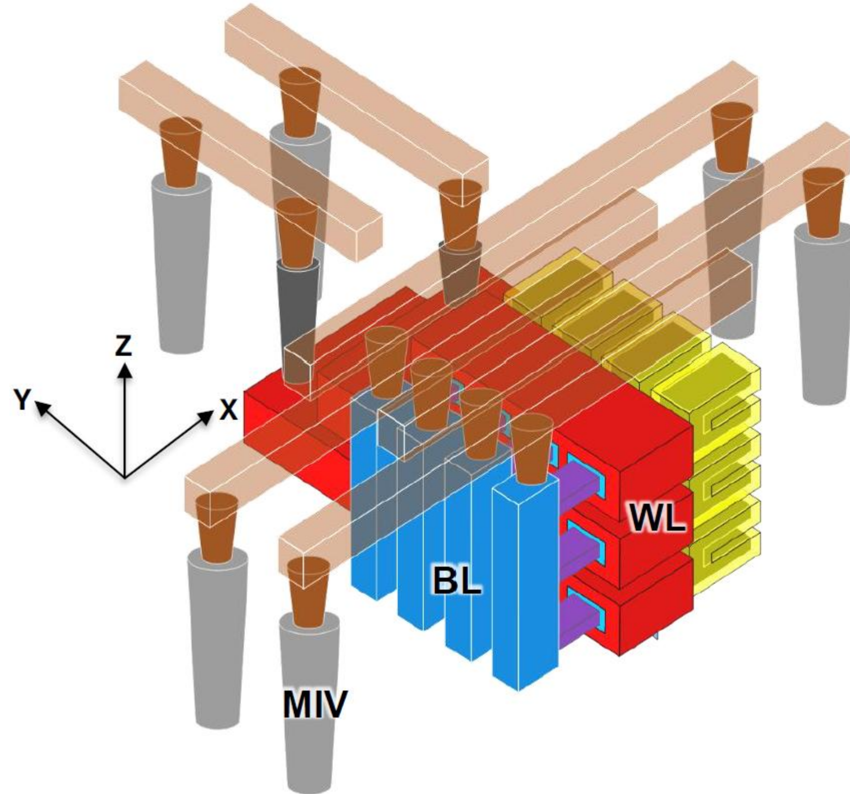
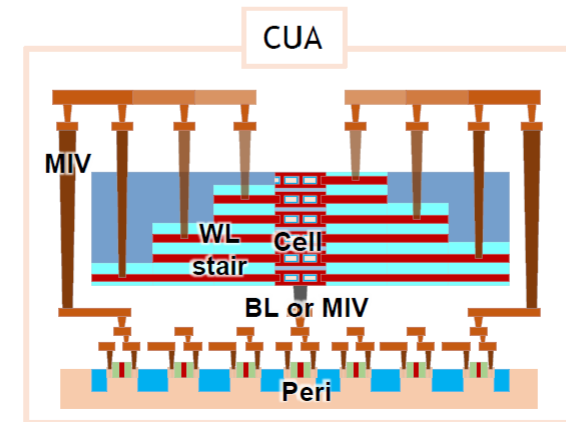


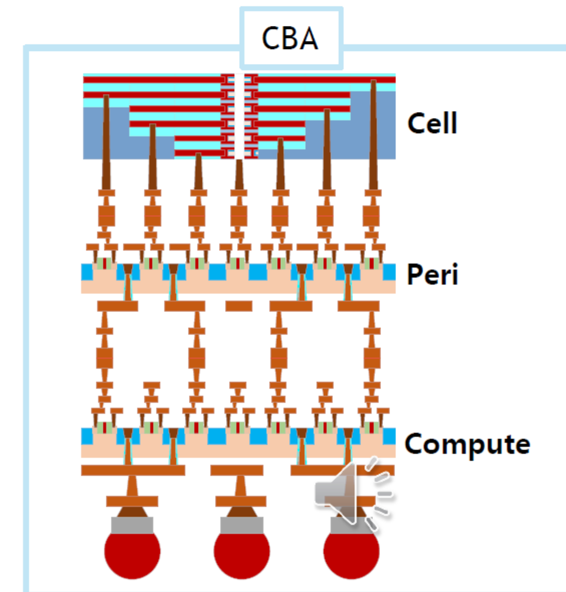
Fig. 12. Memory Window as a function of cycles for two different workloads at -2σ. Workload B on the right is the worst-case workload identified in [2].

A. Calderoni *et al*., "**Voltage Reduction (1.4V) and Array Scaling (41nm)** of Ferroelectric NVDRAM for Low-Power and High-Density Applications," paper 6-2, *2025 Symp. VLSI.* [Micron]

BiCS-Type Horizontally Stacked Fe Cap







E. Sarkar et al., paper T11-2, Symp. VLSI 2026 [Georgia Tech.]

BiCS-Type Horizontally Stacked Fe Cap

BiCS Flow: 3D FeRAM

(1) Mold (Si/SiO_2) → Device isolation

(2) Plate/BL trench → Si release

(3) WL formation

(4) Capacitor / Plate

(5) IGO replacement

(6) BL Formation

Si
SL
IGO
Plate
BL
SiO_2
WL
HfO_2
HZO

Plate trench
BL trench
Staircase
Z X Y

WL X-Section

Tier4 WL4 WL4 IGO 4 20nm Isolation 3
Tier3 WL3 WL3 IGO 3 Isolation 2
Tier2 WL2 WL2 IGO2 Isolation 1
Tier1 WL1 WL1 IGO 1
Pd(WL) Hf Isolation

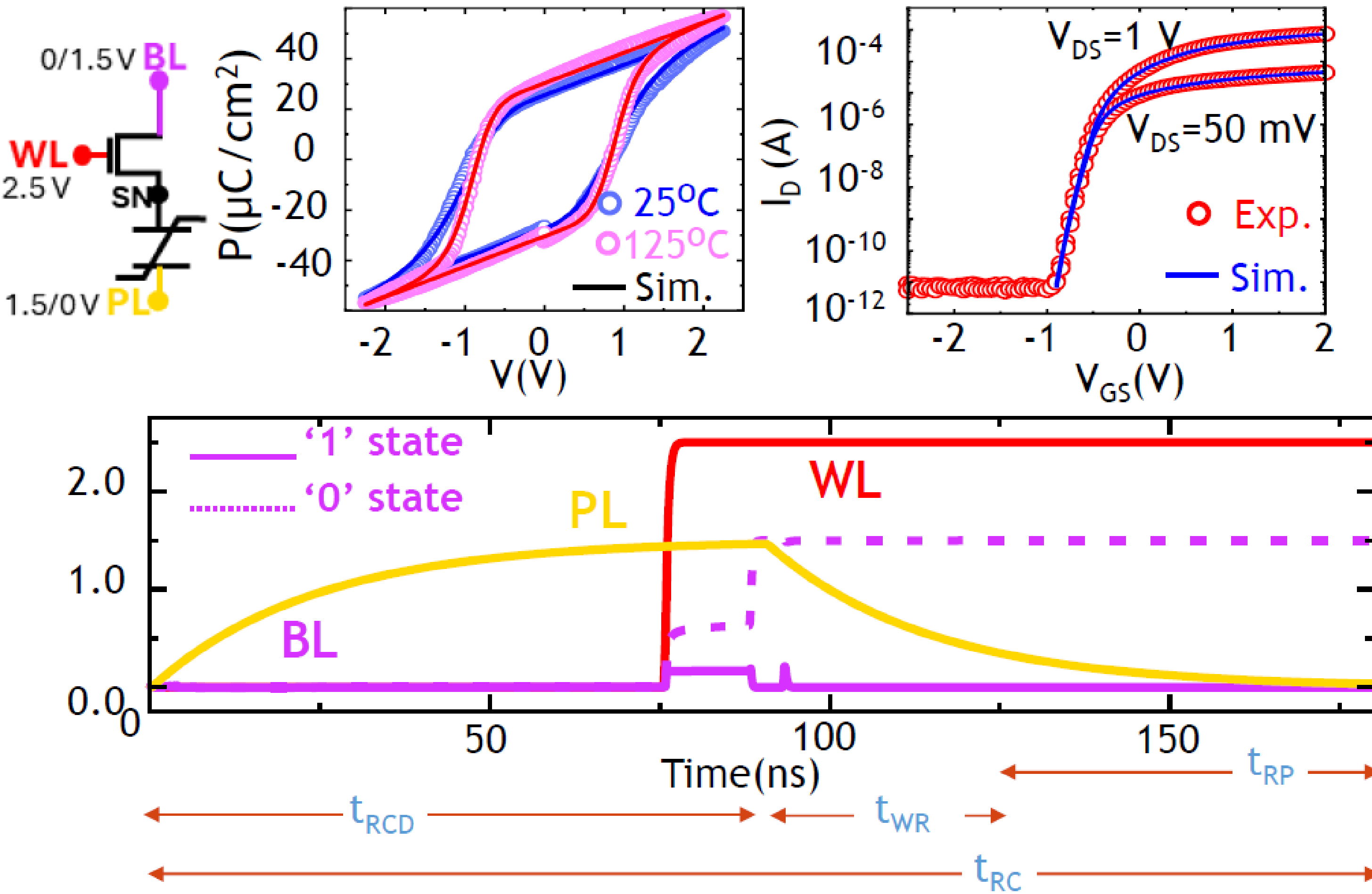
BL X-Section

20nm
BL4 Isolation 3 BL3 Isolation 2 BL2 Isolation 1 BL1
Pd(BL) In, Ga

- BiCS (Bit Cost Scalable) -inspired flow enables monolithic vertical FeRAM integration.

E. Sarkar et al., paper T11-2, Symp. VLSI 2026 [Georgia Tech.]

BiCS-Type Horizontally Stacked Fe Cap



	LPDDR5[2]	NVDRAM[2]	This work
t_{RC}	60 ns	185 ns	180 ns
t_{RCD}	18 ns	85 ns	90 ns
t_{WR}	34 ns	10 ns	27 ns
t_{RP}	18 ns	80 ns	63 ns

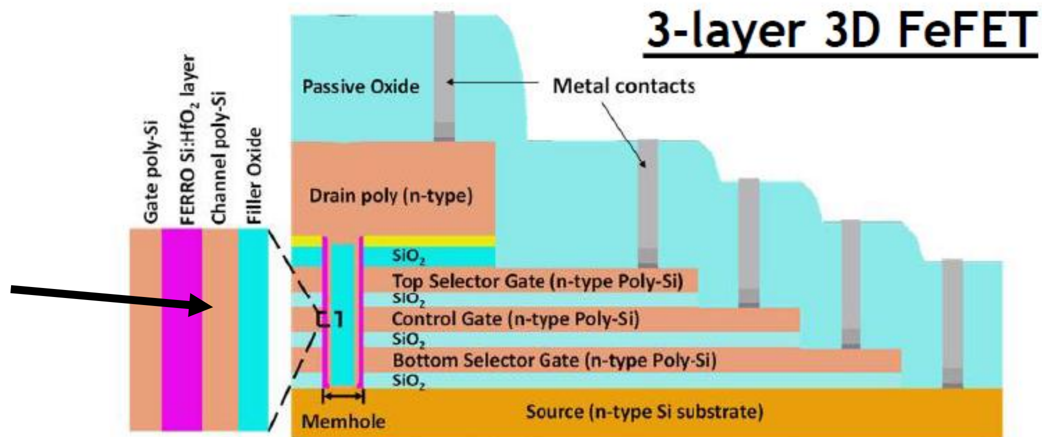
- FeRAM is slower than leading DRAM primarily because plate-line toggling adds extra delay to the read/write operation.

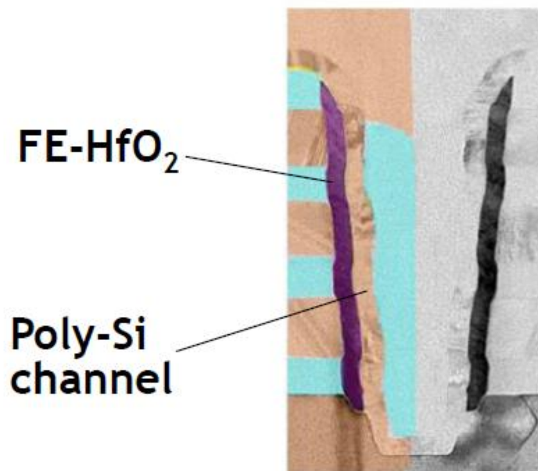
E. Sarkar et al., paper T11-2, Symp. VLSI 2026 [Georgia Tech.]

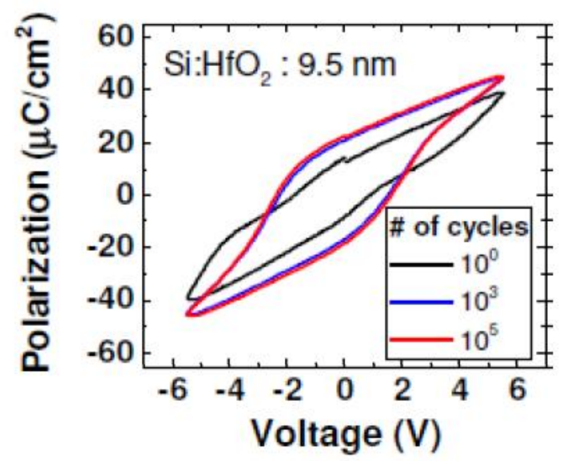
3D Ferroelectric FET ~ 8 Years Ago

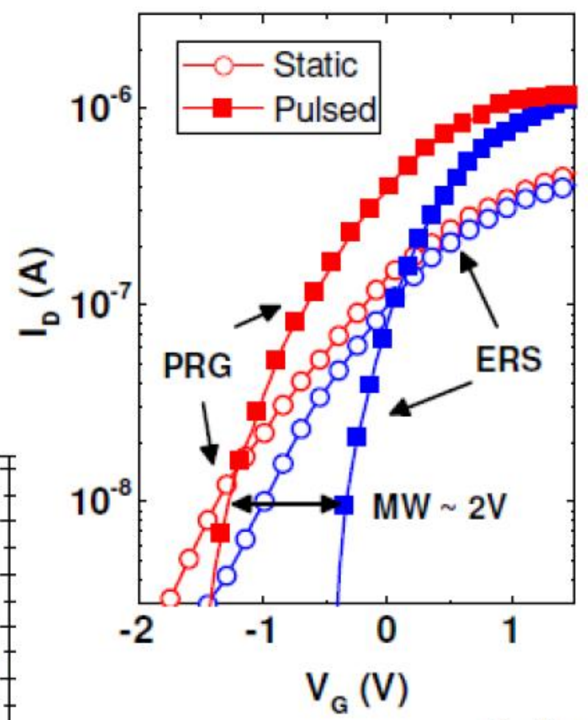
- PolySi FeFET channel

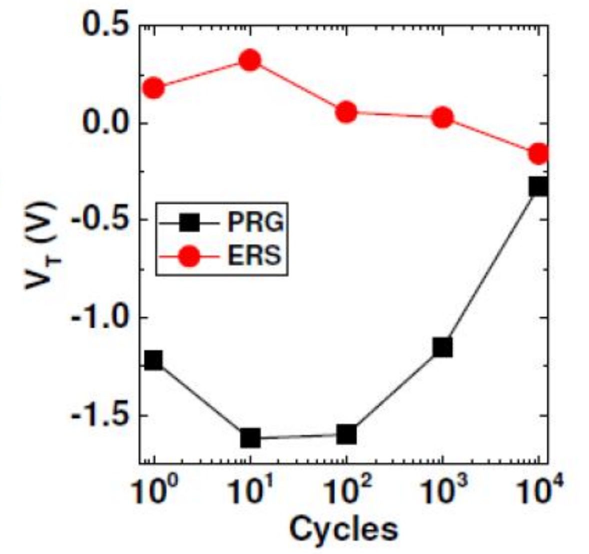
HfO_2 FeFET in 3D flash memory structures (FE-HfO_2 instead of MONOS)









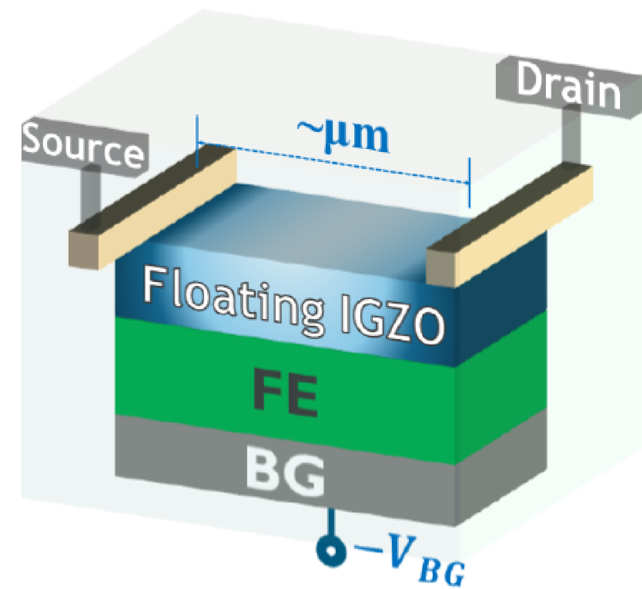


K. Florent et al., IEDM2018, p.43 © 2018 IEEE [59]

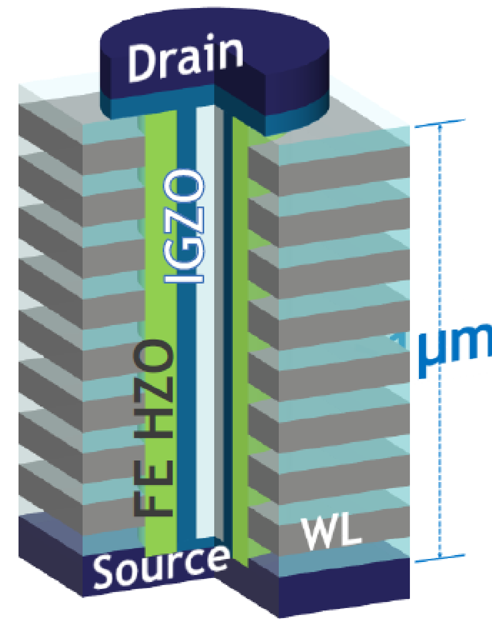
- Due to endurance issue, most FeFET works use oxide channels recently

M. Saitoh (Kioxia), "Key device technology and challenges for 3D non-volatile memory," Symp. VLSI Short Course, 2021.

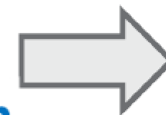
3D Vertical FeFET (NAND)

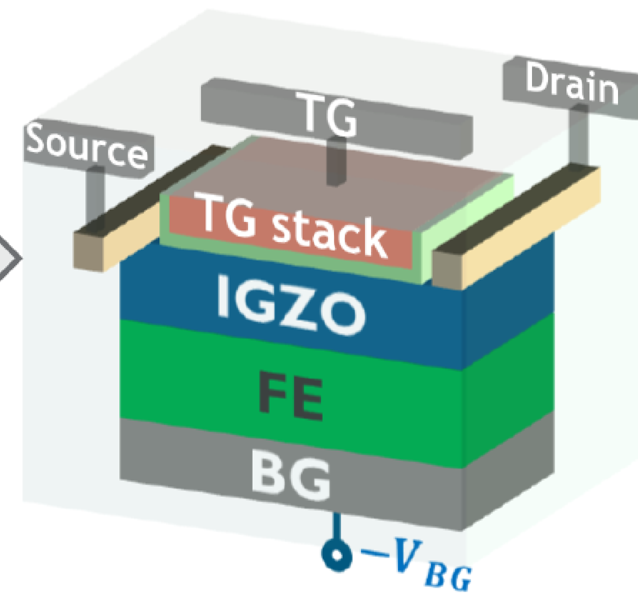


Singl-Gate (SG) FeFET

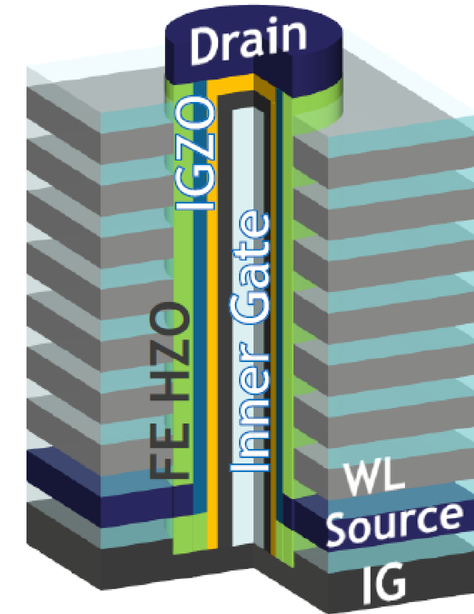


3D FeFET





Dual-Gate (DG) FeFET



3D-DG FeFET

Z. Chen et al., paper T18-5, Symp. VLSI 2026 [IMEC]

3D Vertical FeFET (NAND)

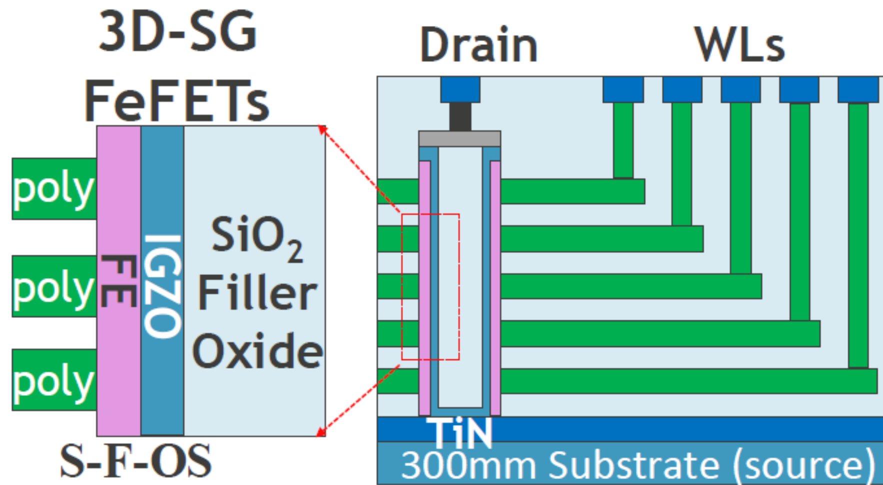
	SLC NAND flash	IGZO-channel FeFET
3D-stacking compatibility	**High**	**High**
Write energy	High	**Low**
Write voltage	High	**Low**
Endurance	$< 10^5$	**$\geq 10^8$ (IL-free)**
Update latency	100μs~ms	**~μs (Erase limited)**

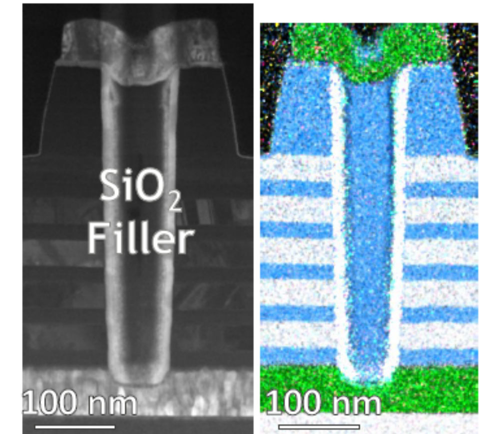
- > 5V write, 100 ns program, 10 μs erase

Z. Chen et al., paper T18-5, Symp. VLSI 2026 [IMEC]

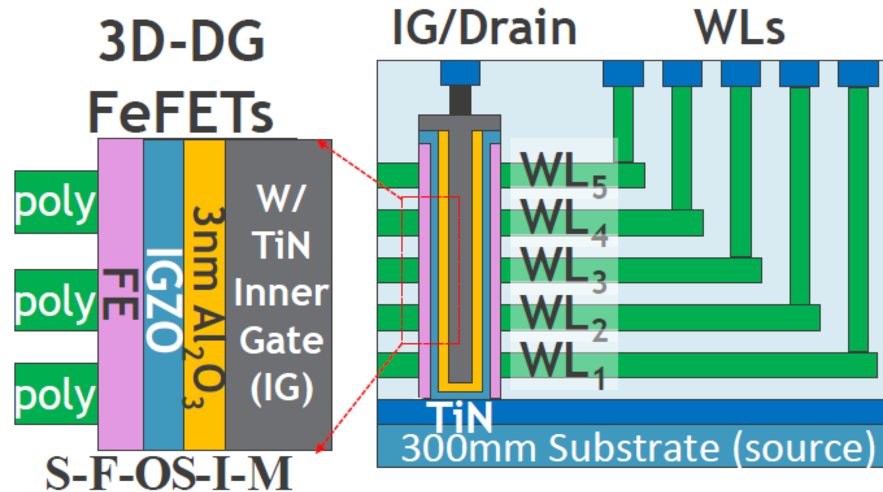
3D Vertical FeFET (NAND)

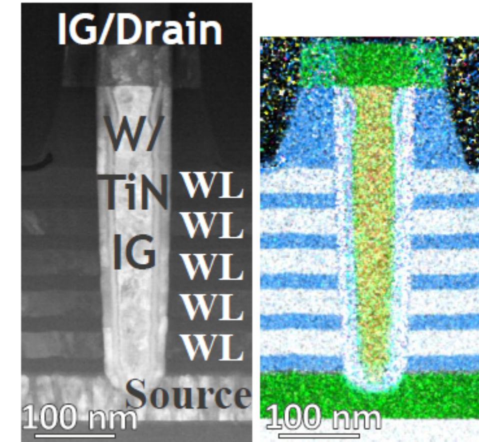
- 3D-SG:
  - Poly-Si/FE/IGZO





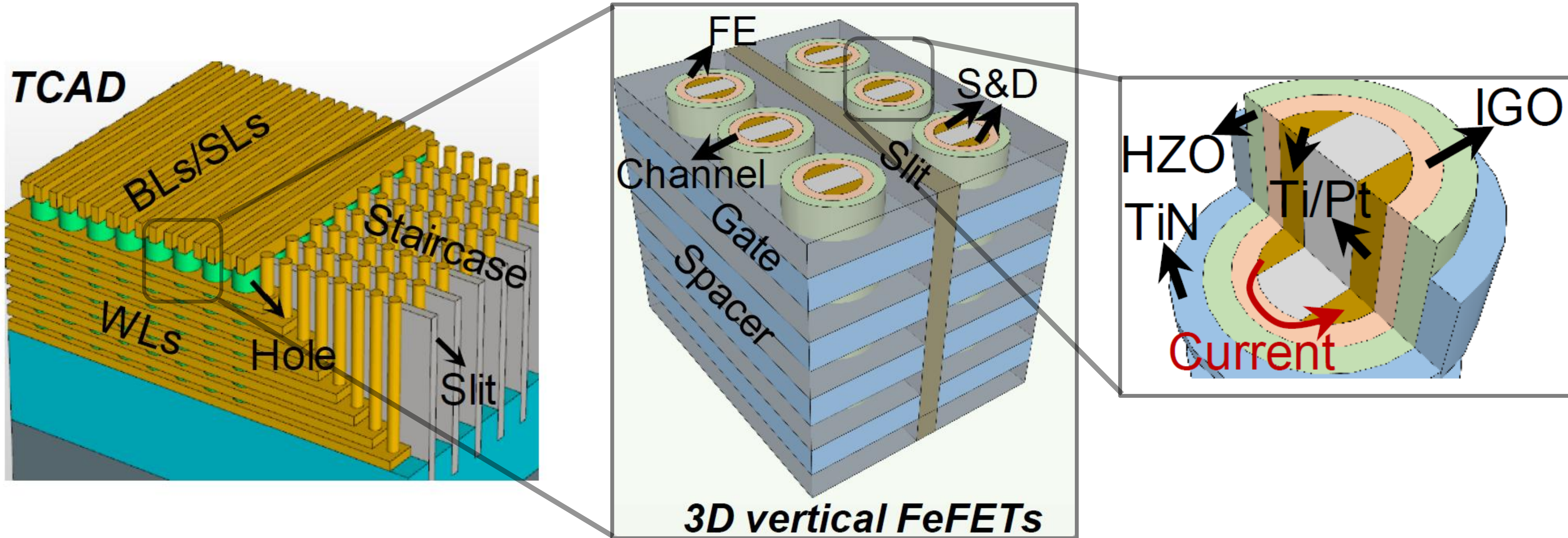
- 3D-DG:
  - Poly-Si/FE/IGZO/Al_2O_3/IG
  - TEM/EDS confirms clean interfaces and uniform layers





Z. Chen et al., paper T18-5, Symp. VLSI 2026 [IMEC]

3D Vertical FeFET (AND)

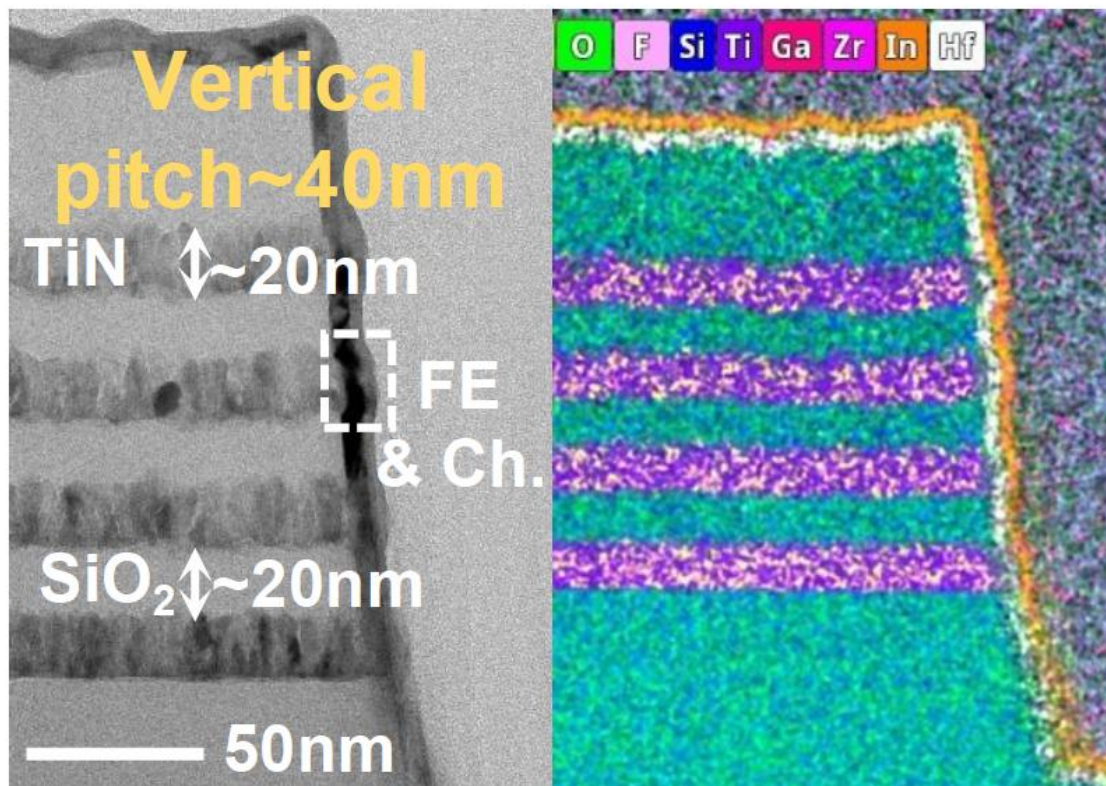


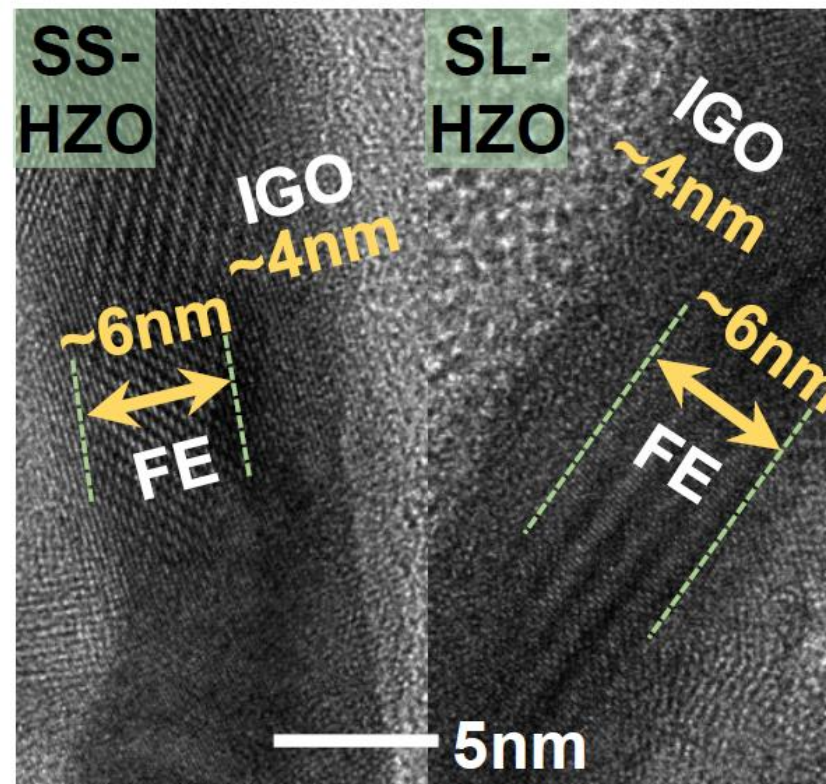
Y. Zhuo et al., paper T1-1, Symp. VLSI 2026. [PKU/YMTC]

3D Vertical FeFET (AND Array)

4-layer 32×32 vertical FeFET array is fabricated

- Aggressively scaled vertical pitch of ~40 nm → Most scaled in 3D FeFETs
- FE and IGO channel thickness scaled to 6/4 nm

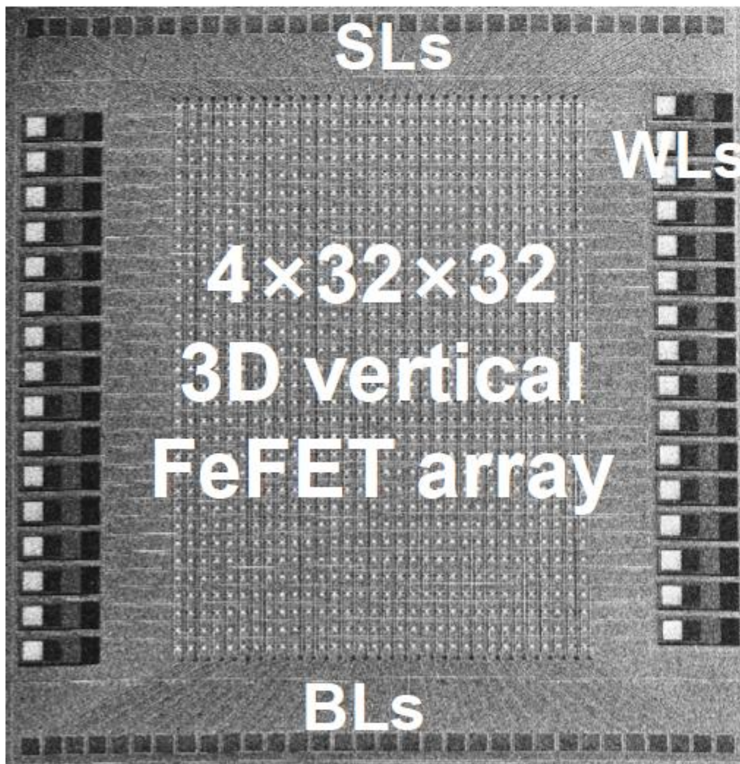


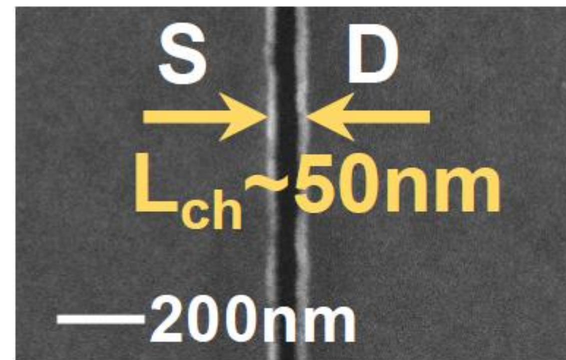


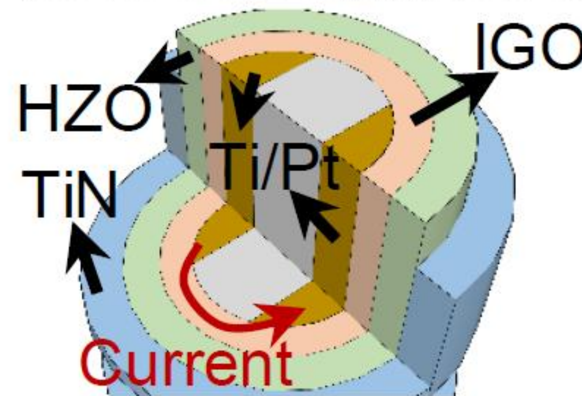
Y. Zhuo et al., paper T1-1, Symp. VLSI 2026. [PKU/YMTC]

3D Vertical FeFET (AND) SOTA

- 4-layer 32×32 vertical FeFET array is fabricated
  - Channel length (L_{ch}) scaled down to 50 nm
  - Various configuration is applied for optimization







- Stacked layers Dep.
- 3D trench etching
- ALD HZO (SS/SL-O1.6s/SL-O0.1s)
- RTA
- ALD IGO (O-rich /O-poor)
- EBL S&D
- Sputter Ti/Pt
- WL staircase

Y. Zhuo et al., paper T1-1, Symp. VLSI 2026. [PKU/YMTC]

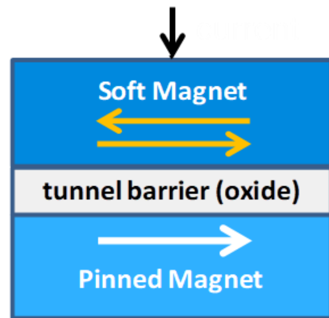
Takeaways

- 1T1C FeRAM
  - Target DRAM-like operations
  - Enduring 1E11-1E12 (at array level) an issue (every read is a write)
  - VDD= 1.4V and lower possible
  - 10s of ns access time
- FeFET
  - Mostly 3D NAND or AND (similar to NOR) structures
  - Oxide semiconductor channels (IGZO, IGO etc.)
  - Mostly conceptual stage with < 10 layers
  - 100 ns write, 10 µs erase, 1E11 cycles at single cell level

“Emerging” Memories

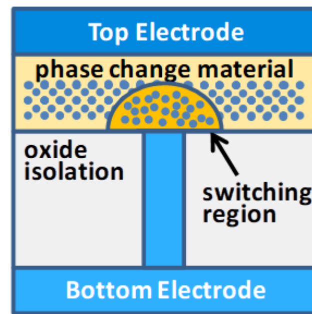
Random access, non-volatile, no erase before write, on-chip integration or cell-bonded to array (CBA)

Some of these already “emerged”



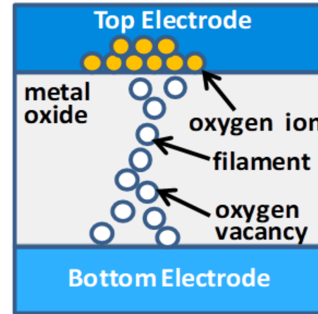
STT-MRAM

Spin transfer torque magnetic random access memory



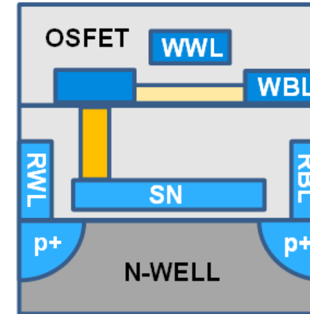
PCM

Phase change memory



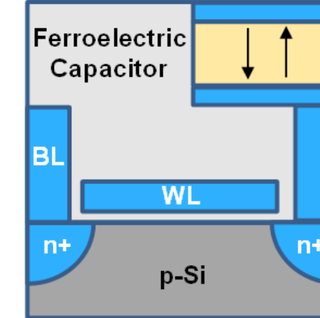
RRAM

Resistive switching random access memory



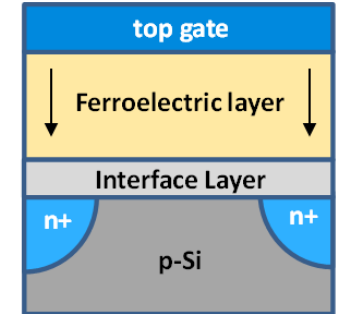
Gain Cell

Gain cell memory (quasi-non-volatile)



FeRAM

Ferro-electric 1T1C memory (destructive read)



FeFET

Ferro-electric field effect transistor

Updated from: H.-S. P. Wong, S. Salahuddin, *Nature Nanotech.*, 2015.