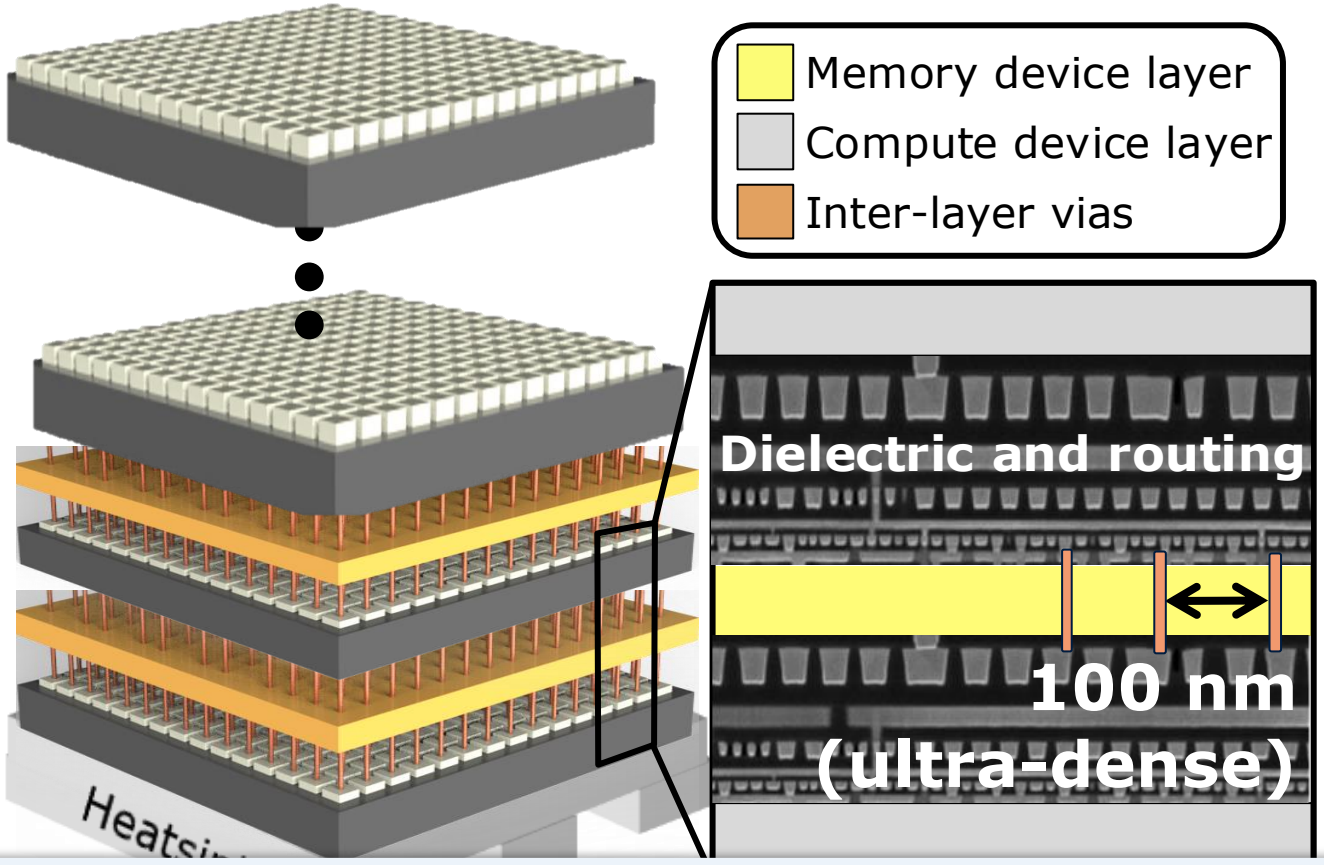
The Future of Cooling 3D ICs

Dennis Rich, Eda Deniz Demirel, Junrui Lyu, Mohamadali Malakoutian, Srabanti Chowdhury, Subhasish Mitra

Visions of Future **Ultra-Dense** 3D ICs

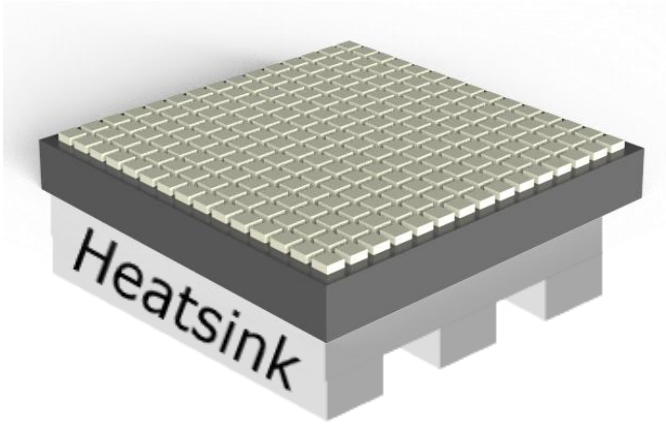


10+ compute tiers, ultra-dense vias

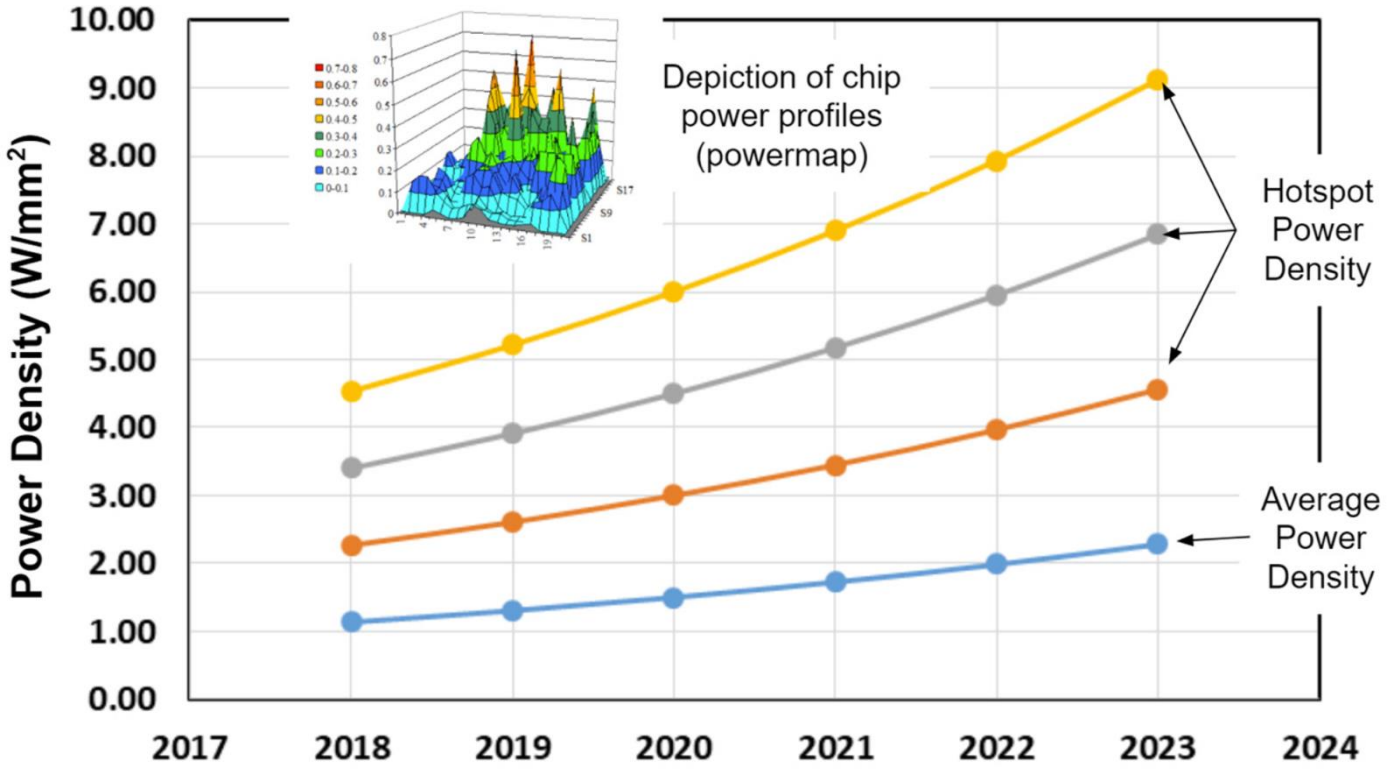
[TSMC, Intel, Stanford]

Conventional Approach to Thermal

AI accelerator cooled by heatsink



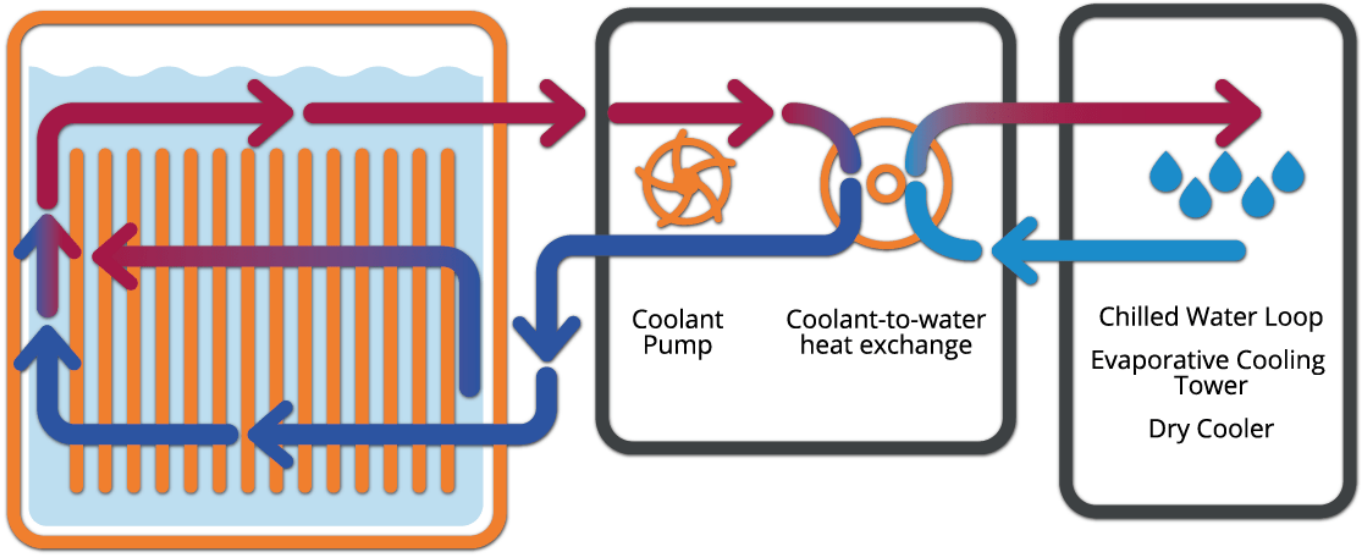
Better heatsinks → higher power density → higher performance



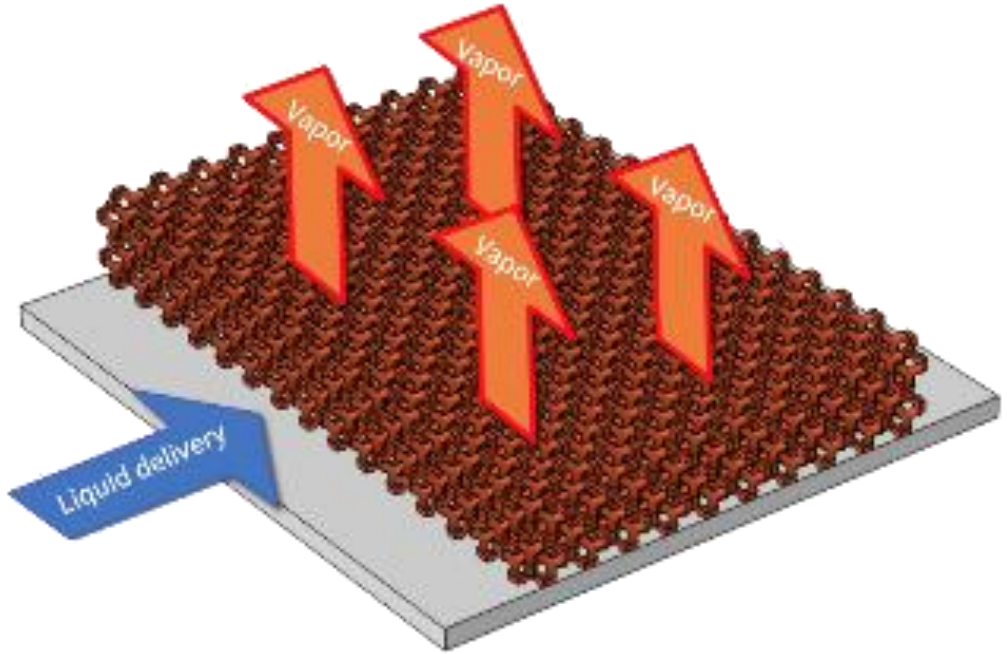
[Heterogeneous Integration Roadmap]

Advanced Heatsinks

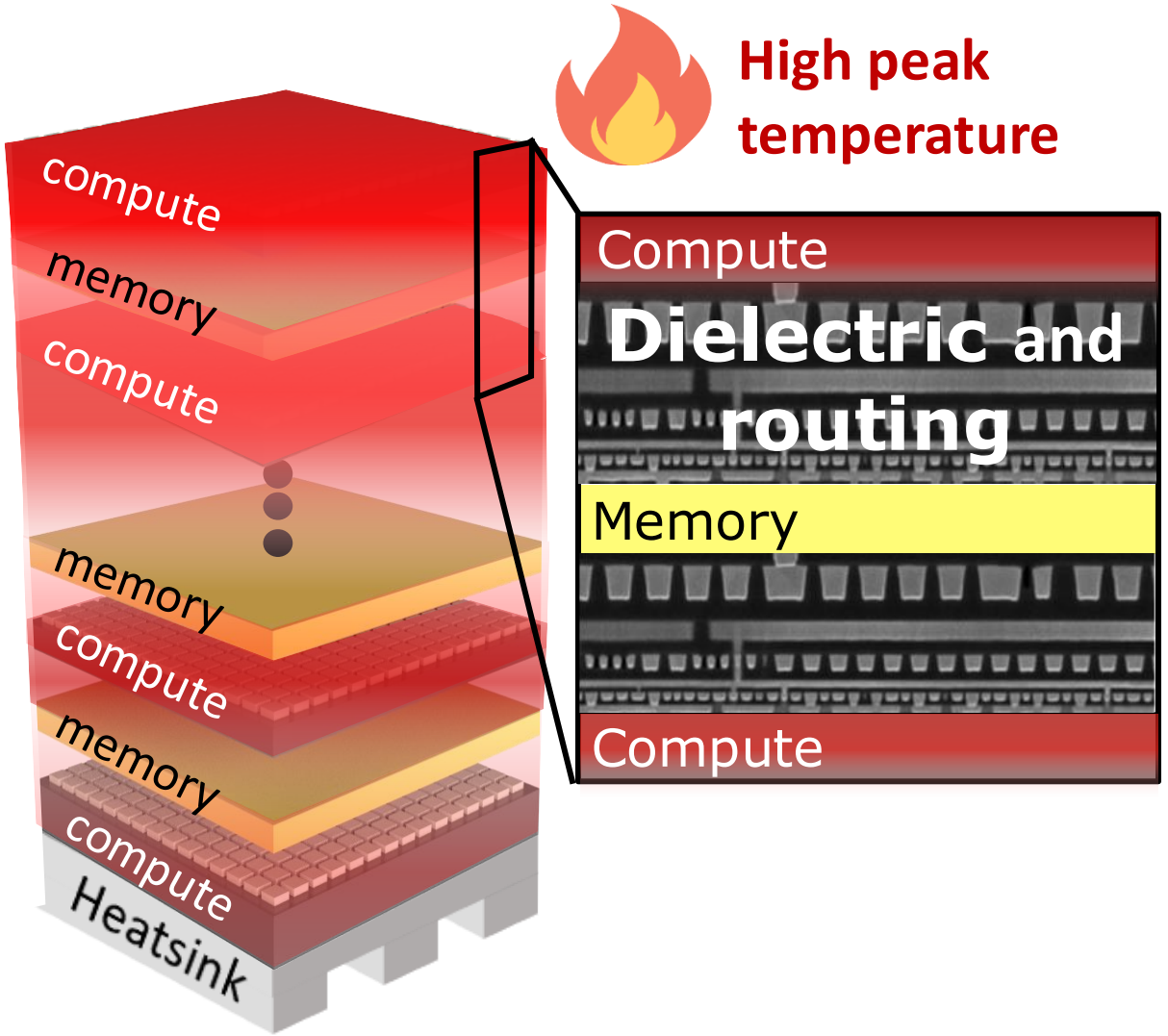
Cryogenic immersion cooling



Two-phase cooling with new materials



3D Thermal



Advanced heatsinks *inadequate*

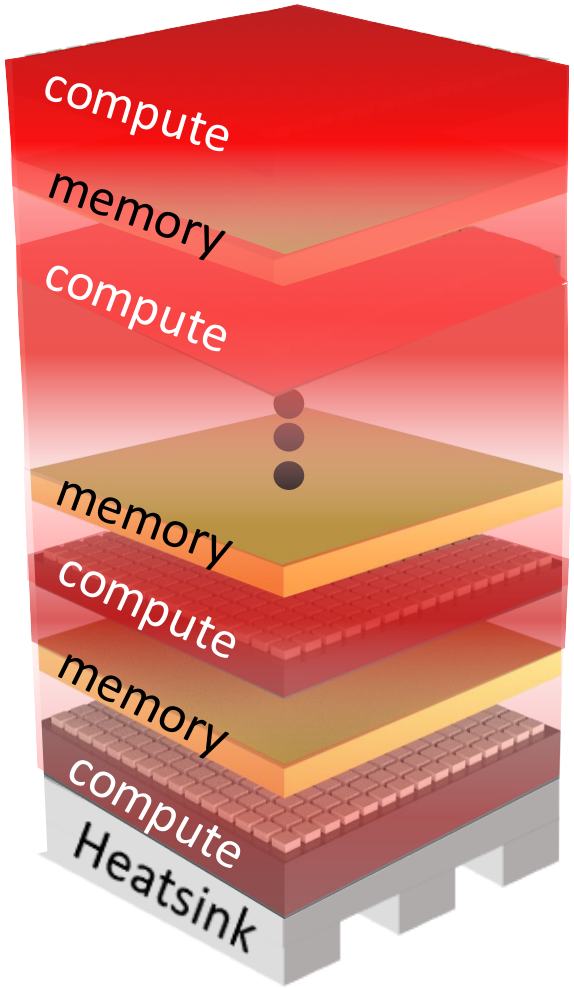
$R_{stack} = 8 \times R_{sink}$

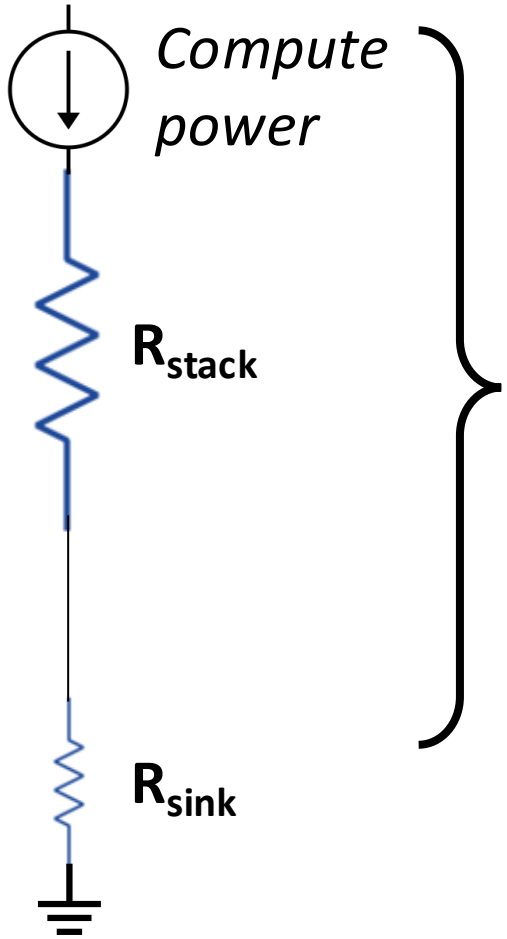
R_{stack} dominates
with just 4 AI accelerator layers in 3D

Low thermal conductivity causes R_{stack} bottleneck

[Rich DAC 23] Copper boiling heatsink = 10^6 W/m^2/K [C. Zhang Adv. Funct. Mater. 18]

3D Thermal





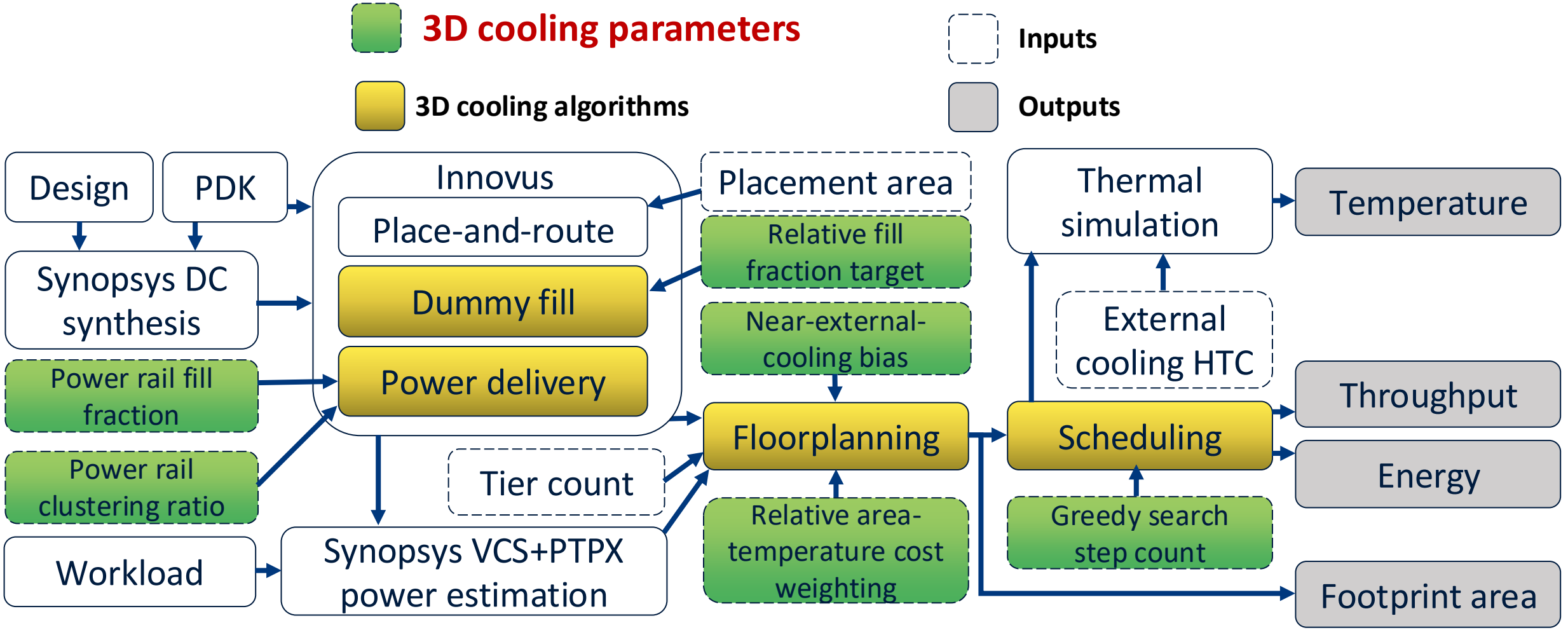
3D Cooling

Existing approaches: Dummy fill, power delivery, floorplanning, scheduling

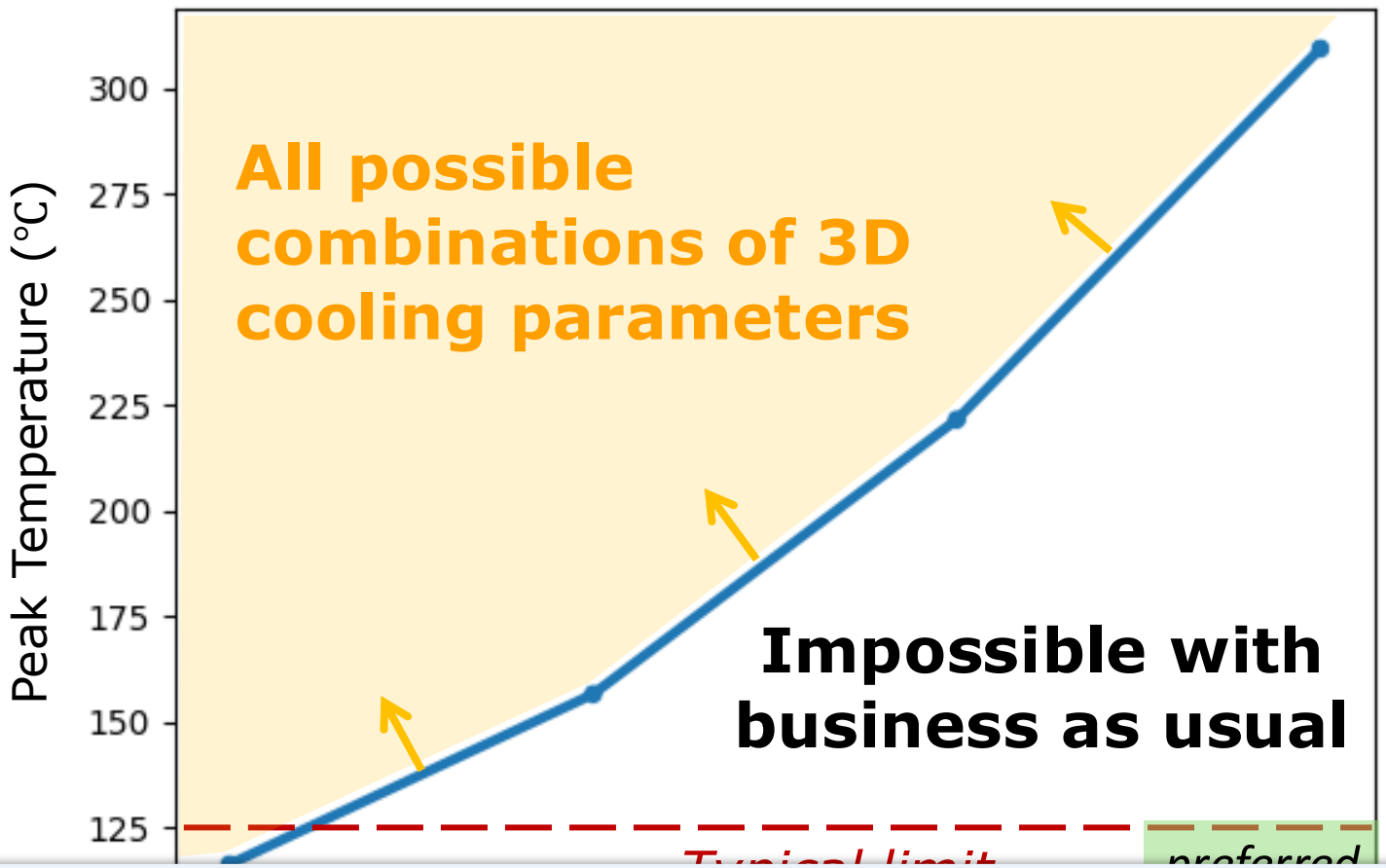
T. Y. Chiang et al., *ICCAD* 2001. J. Cong et al., *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design.*, 2004. H. Wei et al., *IEDM* 2012. J. Li et al., *ACM Trans. Embedd. Comput. Syst.* 2013. S. K. Samal et al., *DAC* 2014. S. K. Samal et al., *IEEE T Compur. Aid D.* 2016. M. A. Iqbal and M. Rahman, *S3S* 2017.

[Rich DAC 23]

Modeling 3D ICs with 3D Cooling



3D Cooling Isn't Good Enough



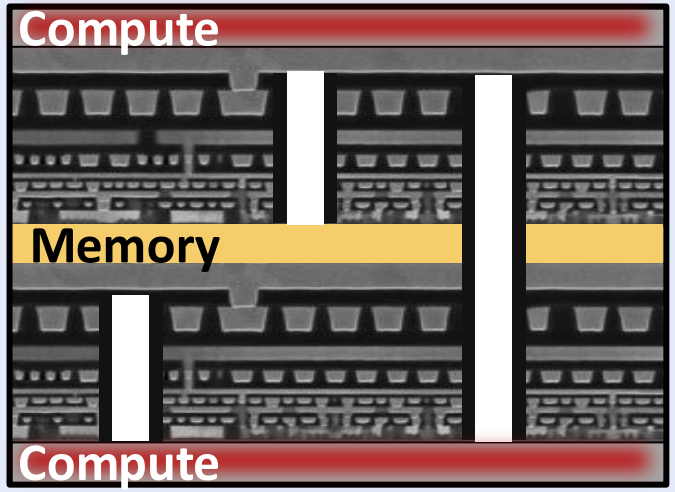
Design Requirements

Metric	Maximum Allowed
Area	1.1× Baseline
Peak Temp	125 °C
Clock Period	1.1× Baseline
Via Pitch	100 nm*

New approaches needed

3D Thermal Scaffolding

Scaffolding Vias



☹ **Area overhead**

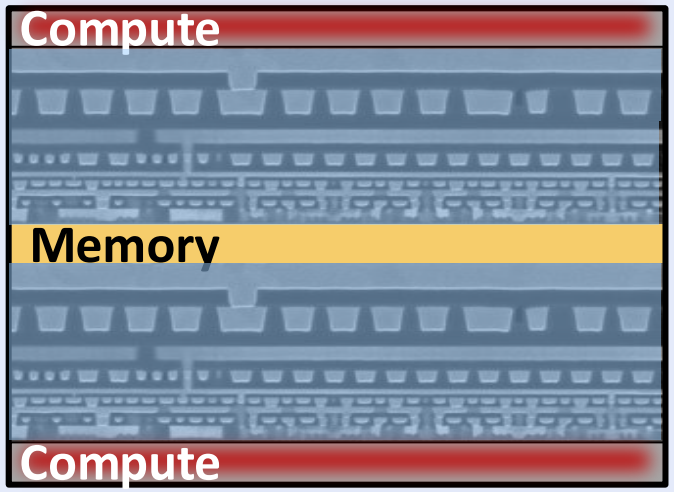
☺ High vertical TC

TC

Thermal conductivity

+

Today's Inter Layer Dielectric



☹ **Low TC**

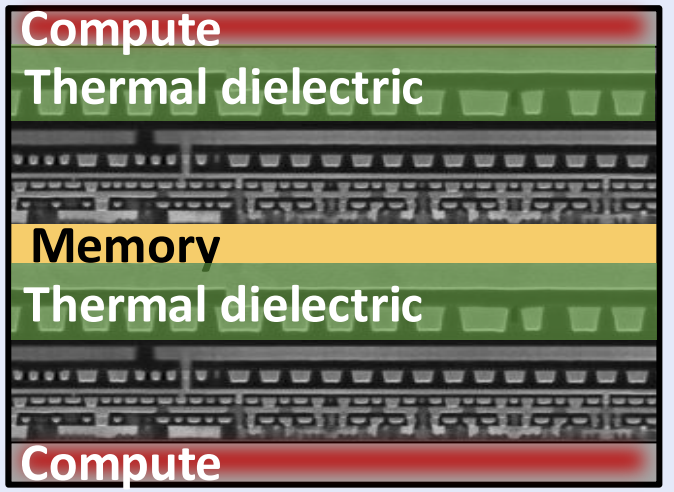
☺ Ultra-low κ

κ

Dielectric constant

+

New Thermal Inter Layer Dielectric



☺ **High lateral TC**

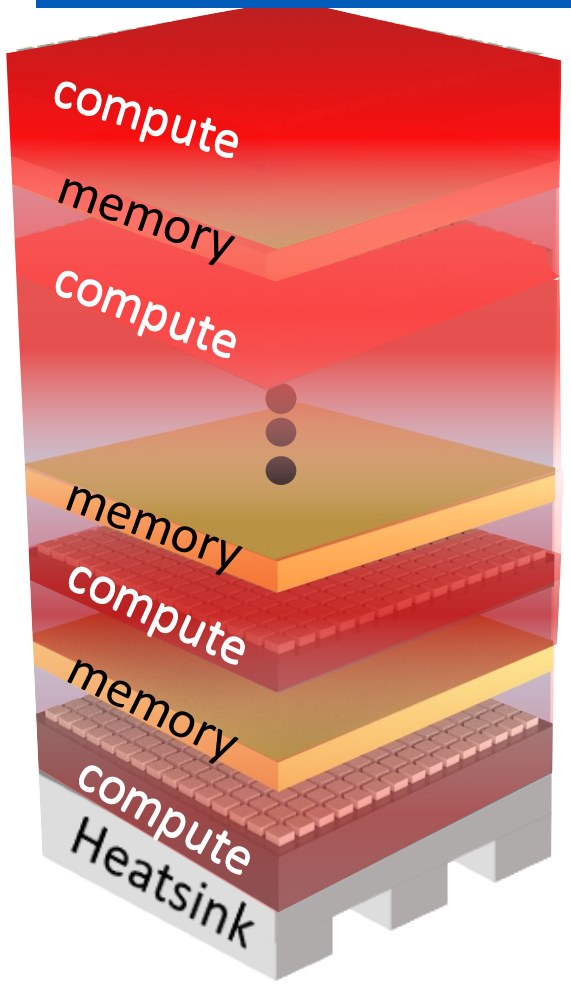
😐 Moderately low κ

Selectively placed

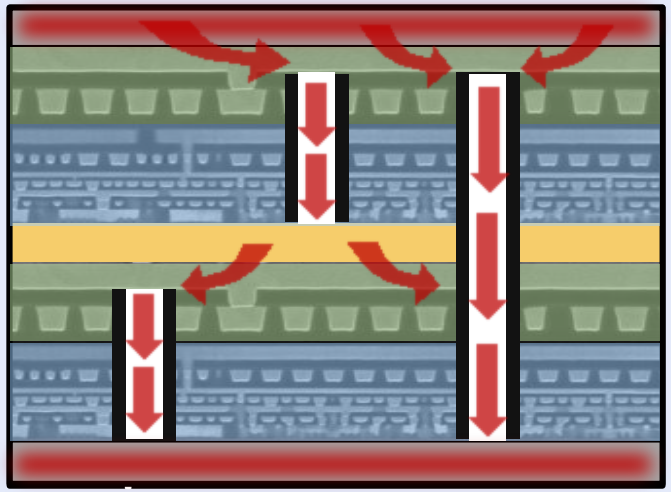
e.g., power routing

Scaffolding via = Normal BEOL metal via used for scaffolding

3D Thermal Scaffolding



Co-placement physical design algorithms



Scaffolding vias

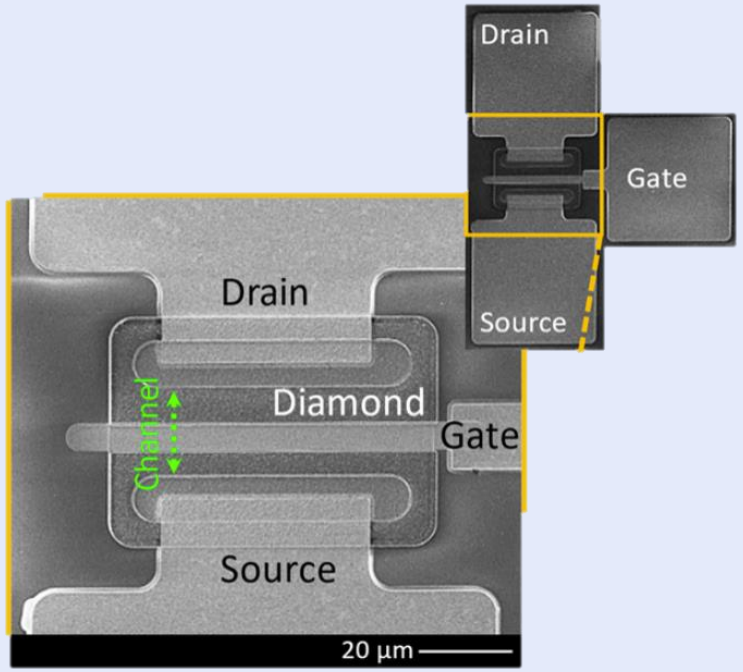
Today's
Inter Layer Dielectric

New Thermal
Inter Layer Dielectric

10× temperature reduction ***unlocked***

Polycrystalline Diamond Thermal Dielectric

Originally used for power transistor cooling



[Malakoutian Cryst. Growth Des. 21]

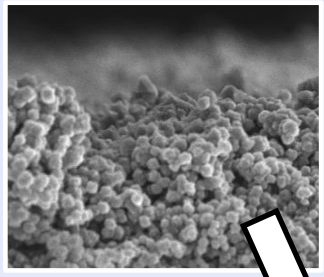
500× better TC vs. today's dielectric

	TC	K
Today's dielectric	~0.2	2
Polycrystalline diamond	105	4

TC = thermal conductivity

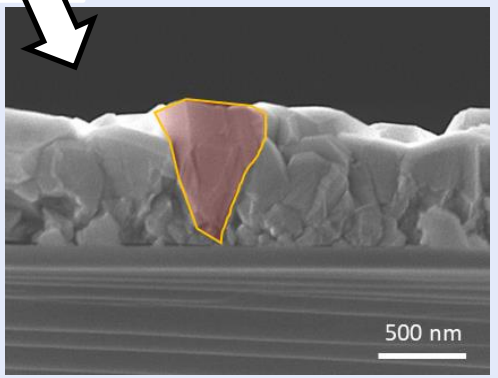
K = dielectric constant (estimated)

≤400°C growth (process-compatible)



H_2 plasma only

O_2 assisted



[Malakoutian Adv. Funct. Mater. 22]

Prof. Srabanti Chowdhury

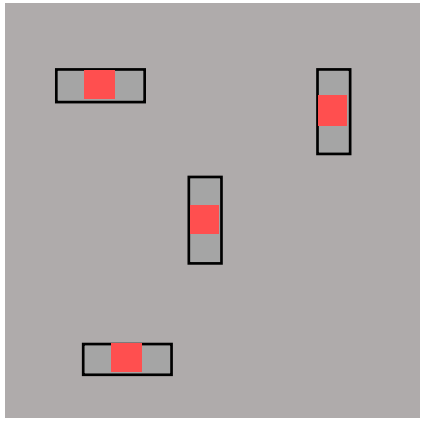
Dr. Mohamadali Malakoutian

Junrui Lyu

Building Scaffolding Step-By-Step

Thermal dielectric
Typical dielectric
Device layer
Copper
Device

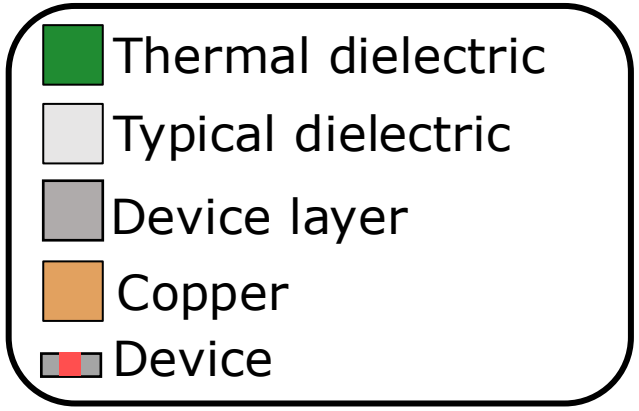
Step 1: Device Fabrication



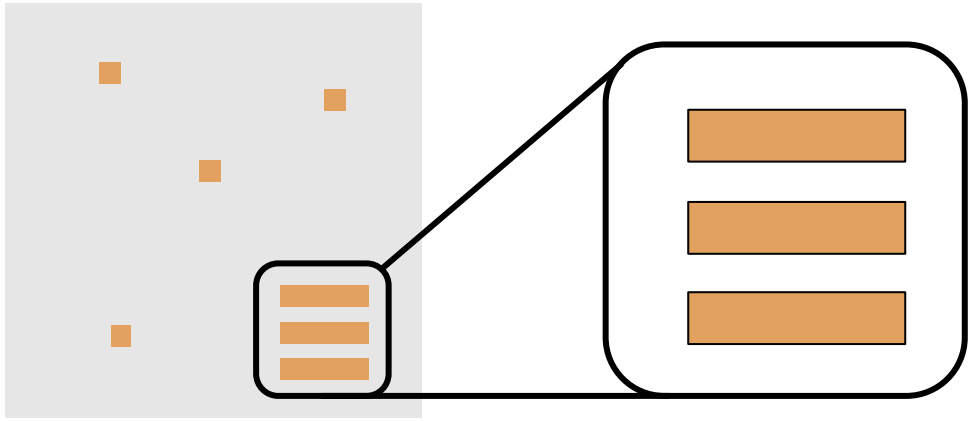
Top view

Side view

Building Scaffolding Step-By-Step



Step 2: Small Vias

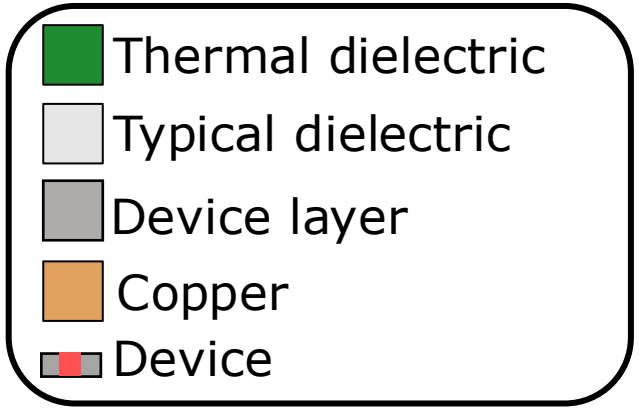


Top view

Scaffolding via

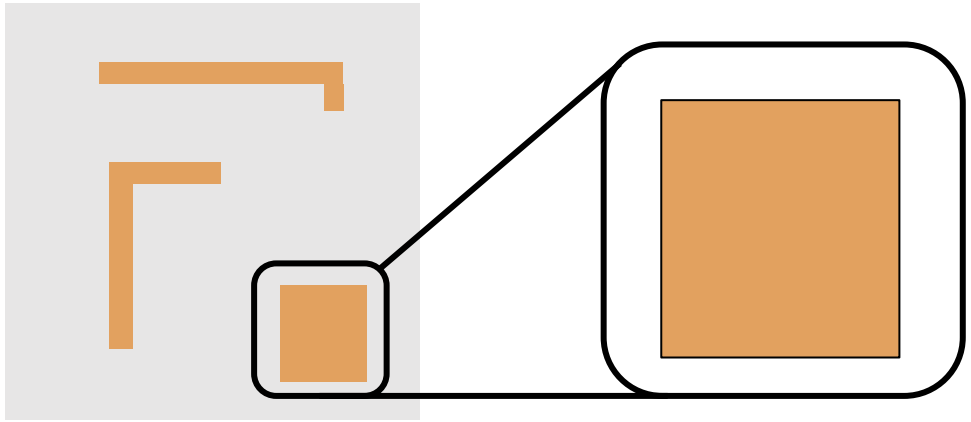
Side view

Building Scaffolding Step-By-Step



Step 3: Small Wires

Typical dielectric minimizes parasitics

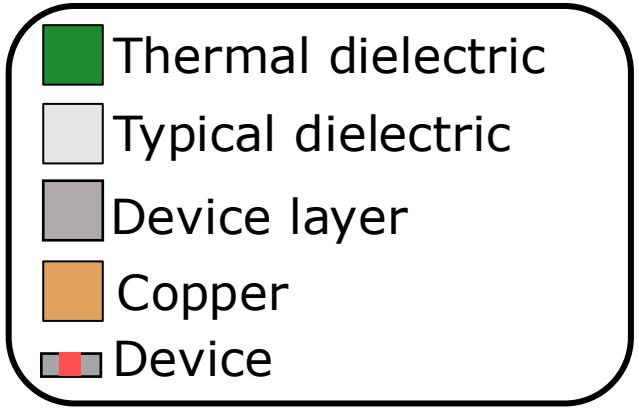


Top view

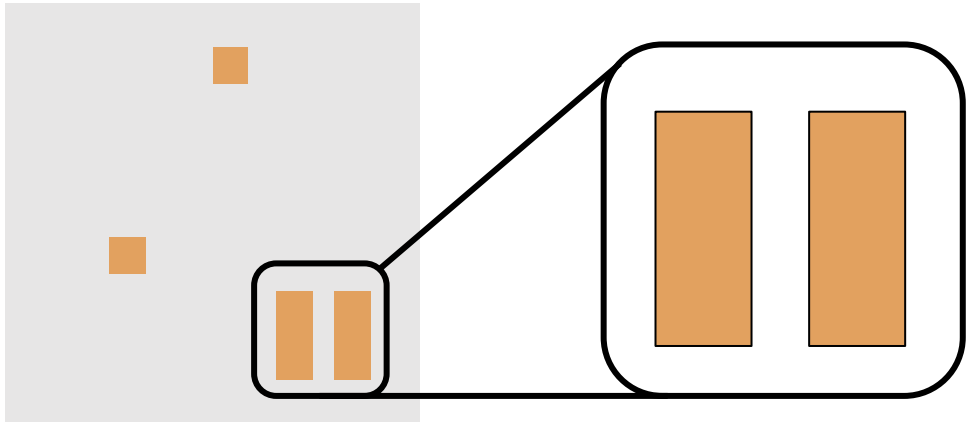
Scaffolding via

Side view

Building Scaffolding Step-By-Step



Step 4: Middle Vias

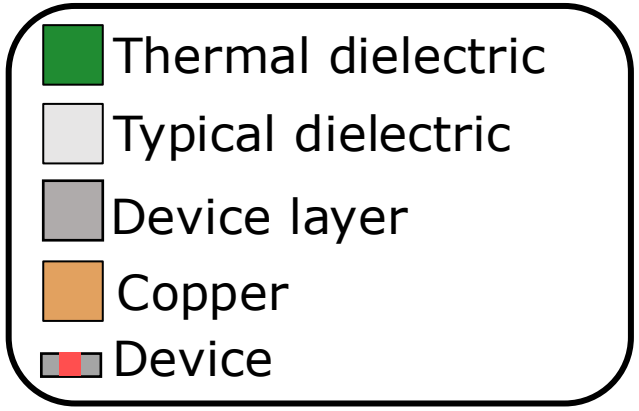


Top view

Scaffolding via

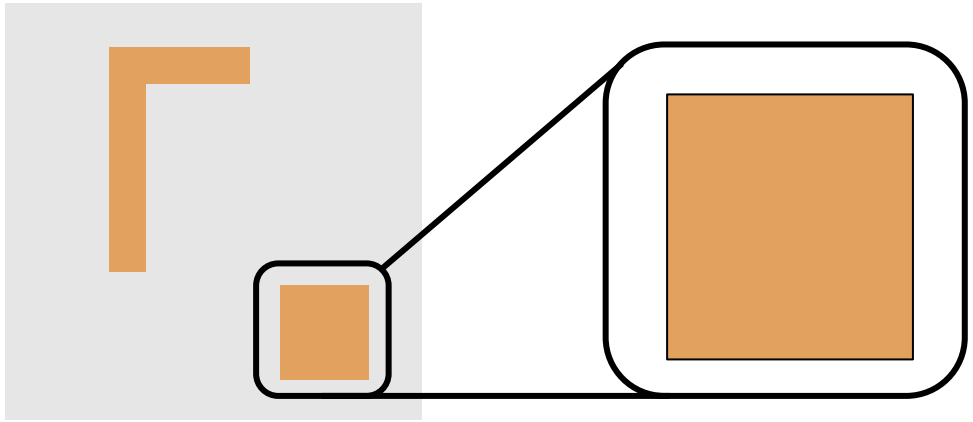
Side view

Building Scaffolding Step-By-Step



Step 5: Middle Wires

Scaffolding vias
follow design rules



Top view Scaffolding via

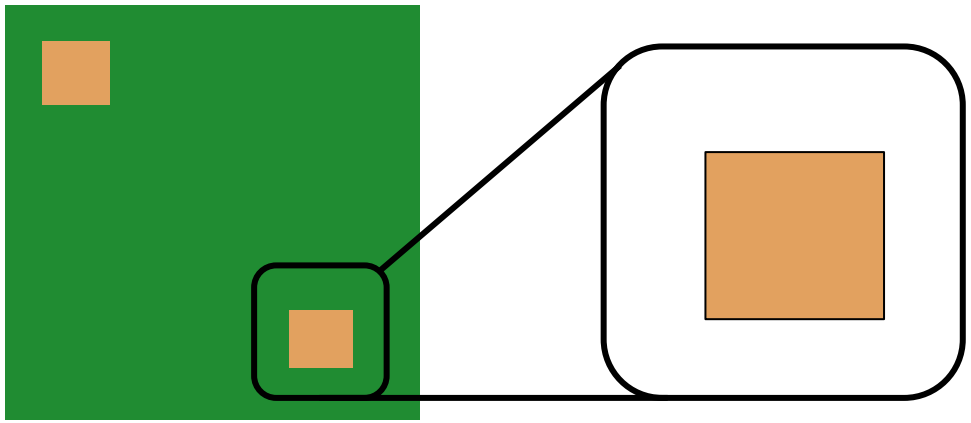
Side view

Building Scaffolding Step-By-Step

Thermal dielectric
Typical dielectric
Device layer
Copper
Device

Step 6: Upper Vias

Upper layers dedicated to power routing



Top view

Scaffolding via

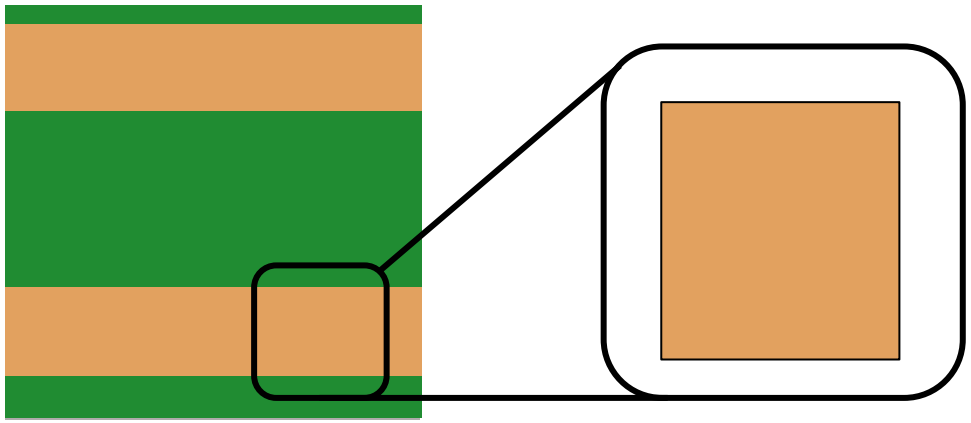
Side view

Building Scaffolding Step-By-Step

Thermal dielectric
Typical dielectric
Device layer
Copper
Device

Step 7: Upper Wires

Scaffolding vias integrated in power routing

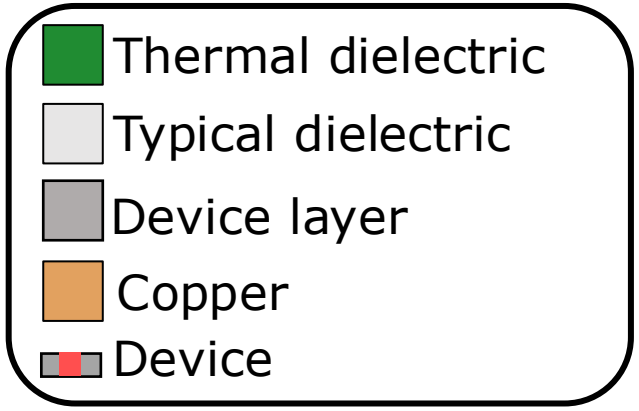


Top view

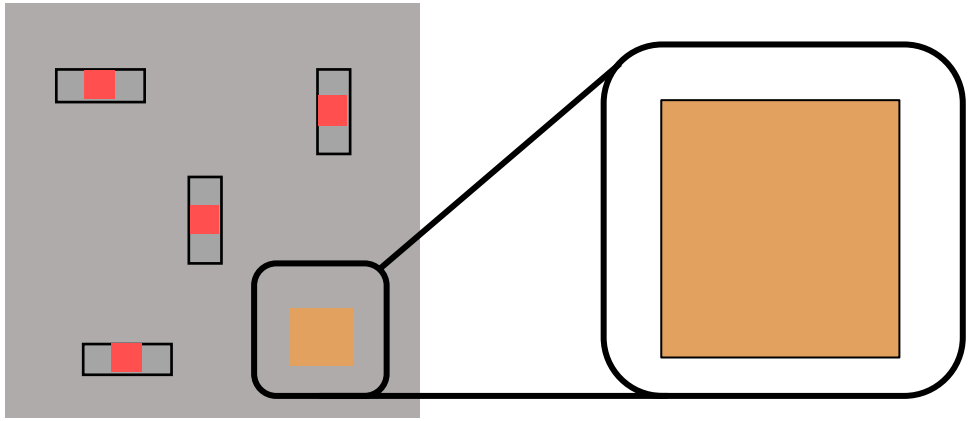
Scaffolding via

Side view

Building Scaffolding Step-By-Step

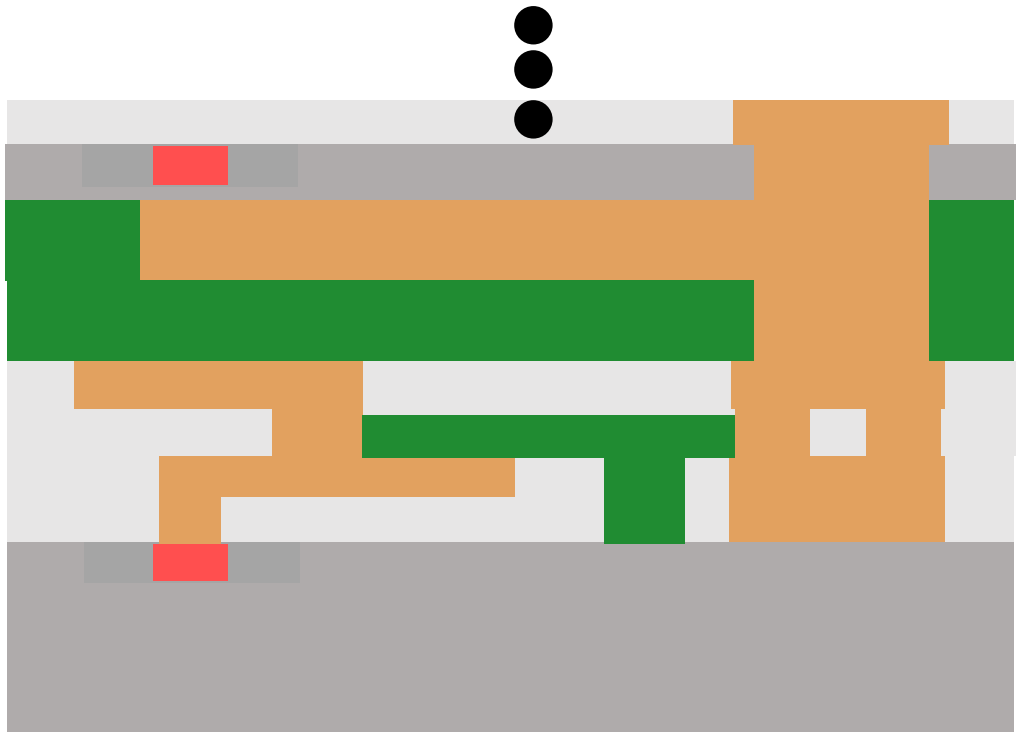


Next: More Devices and Routing



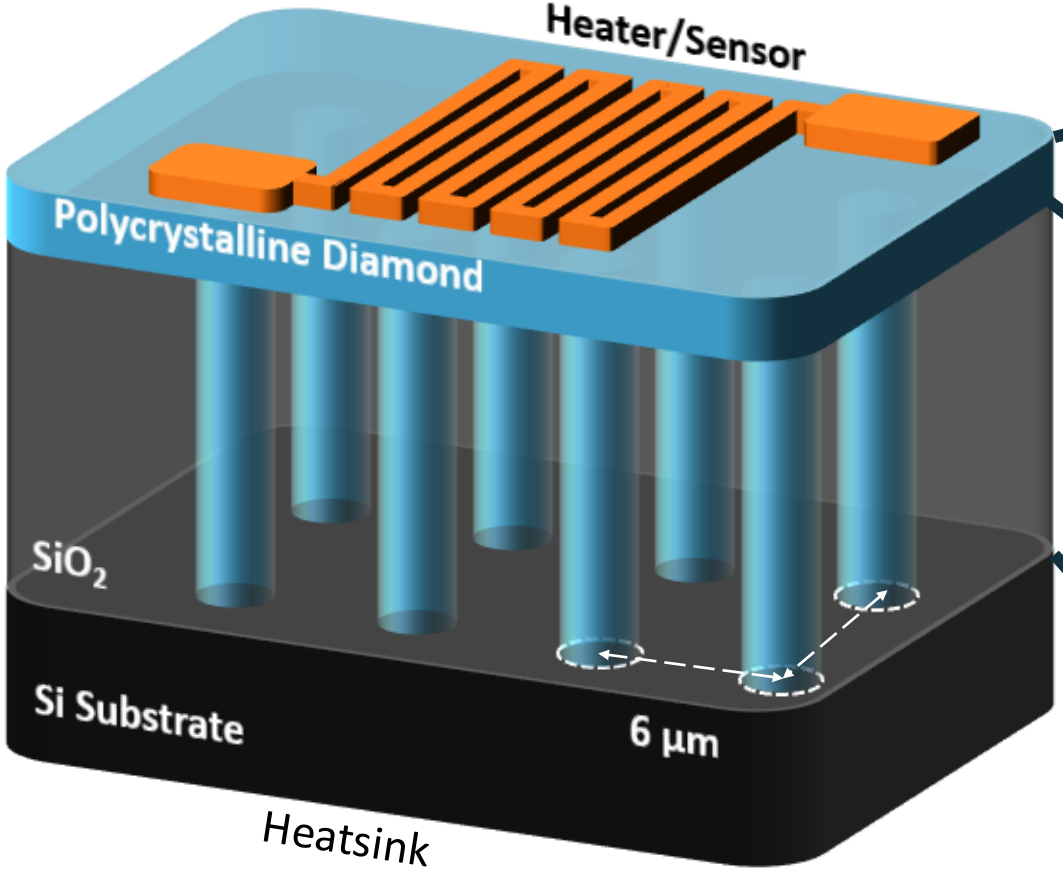
Top view

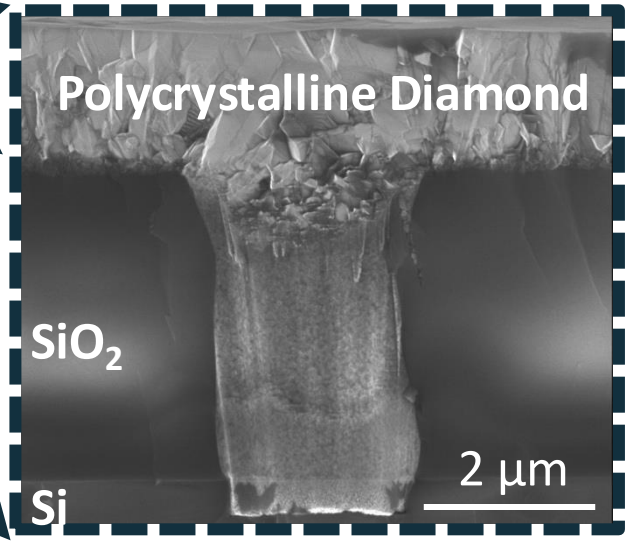
Scaffolding via

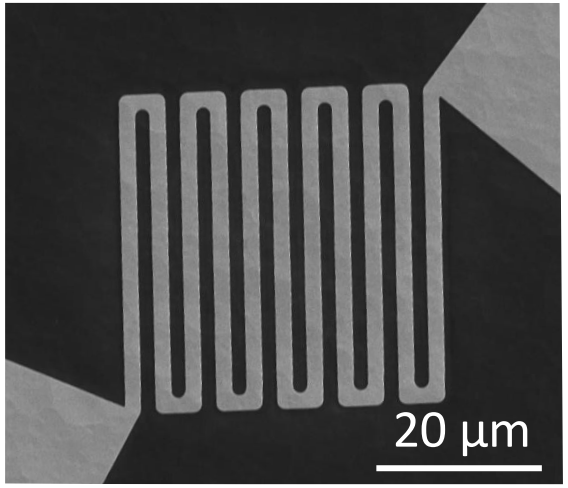


Side view

Large Benefits of 3D Thermal Scaffolding *In Hardware*



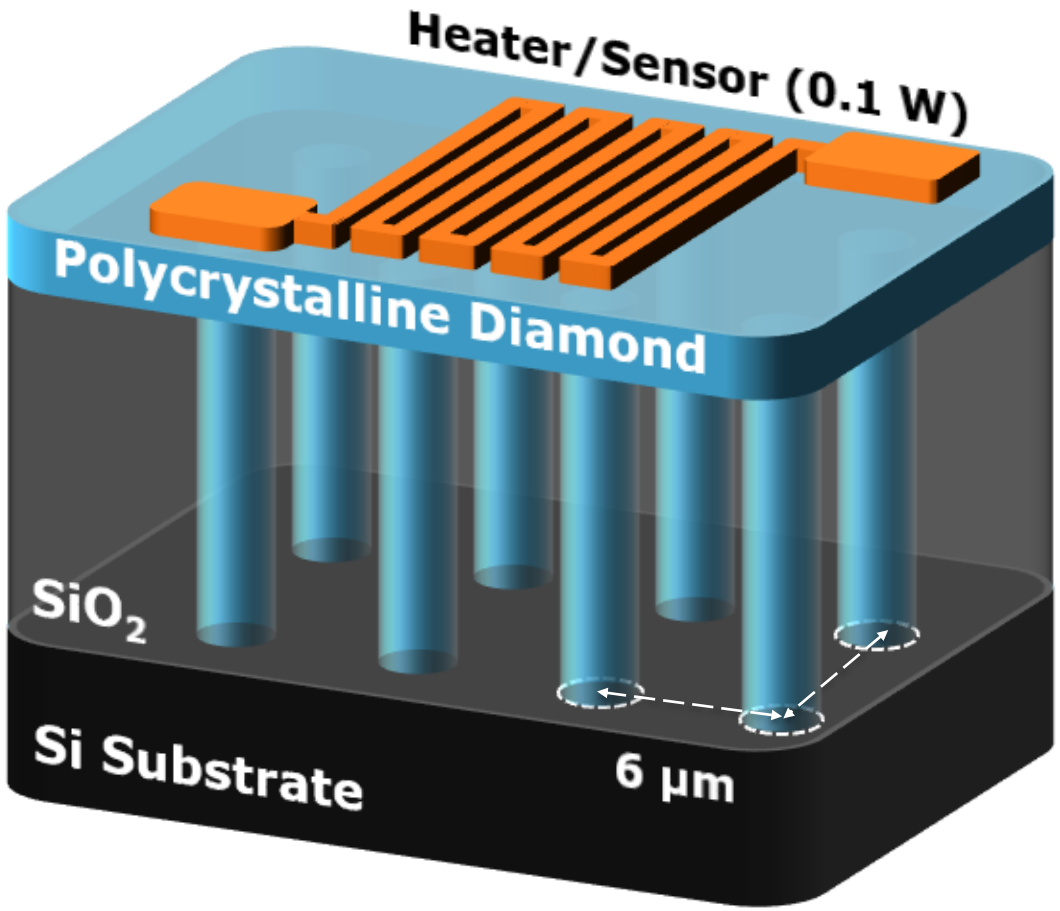


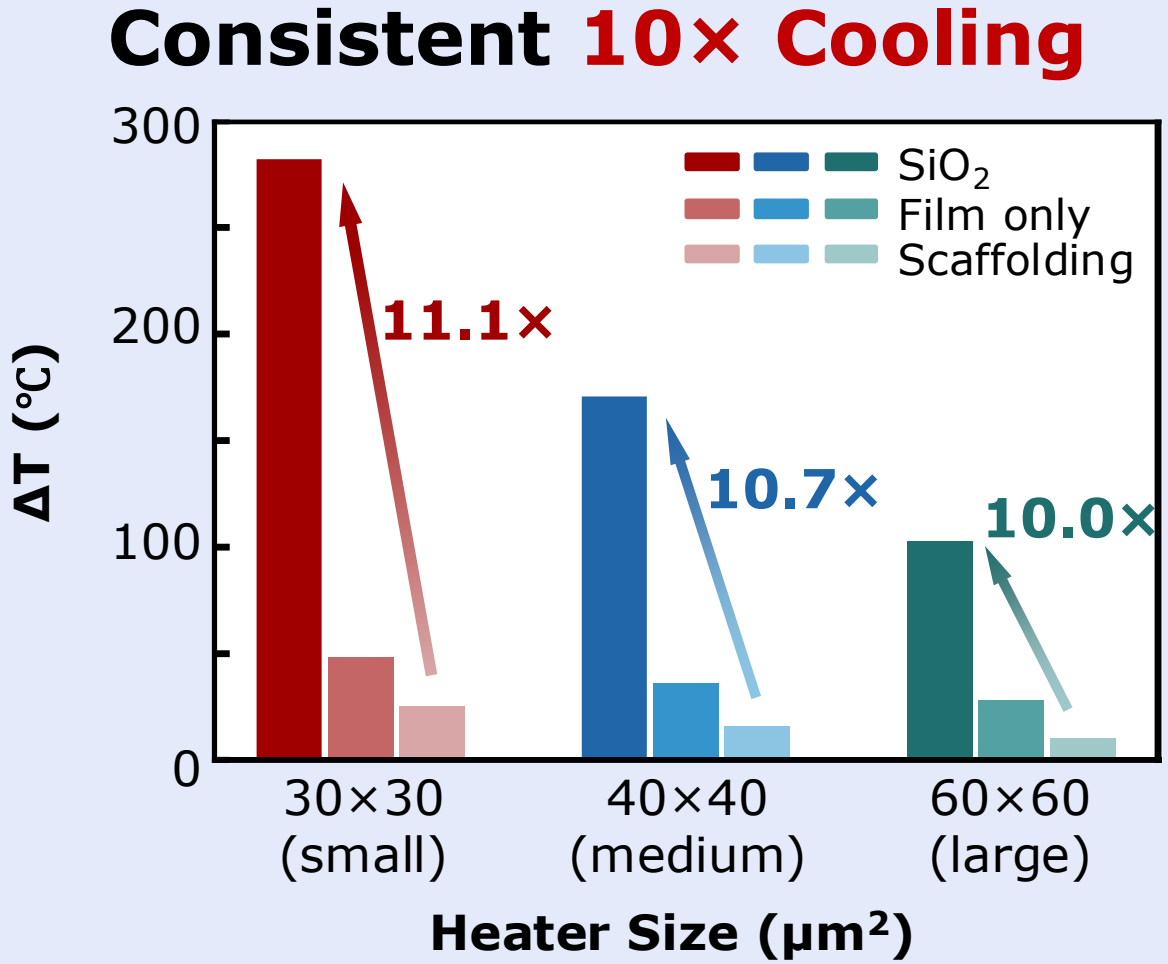


30×30 um² heater at 0.1 W	**SiO_2**	**Scaffolding**
Heater temperature	**304 ℃**	**48 ℃**

[J. Lyu IEDM 2024] Collaborator: Prof. S. Chowdhury (Stanford)

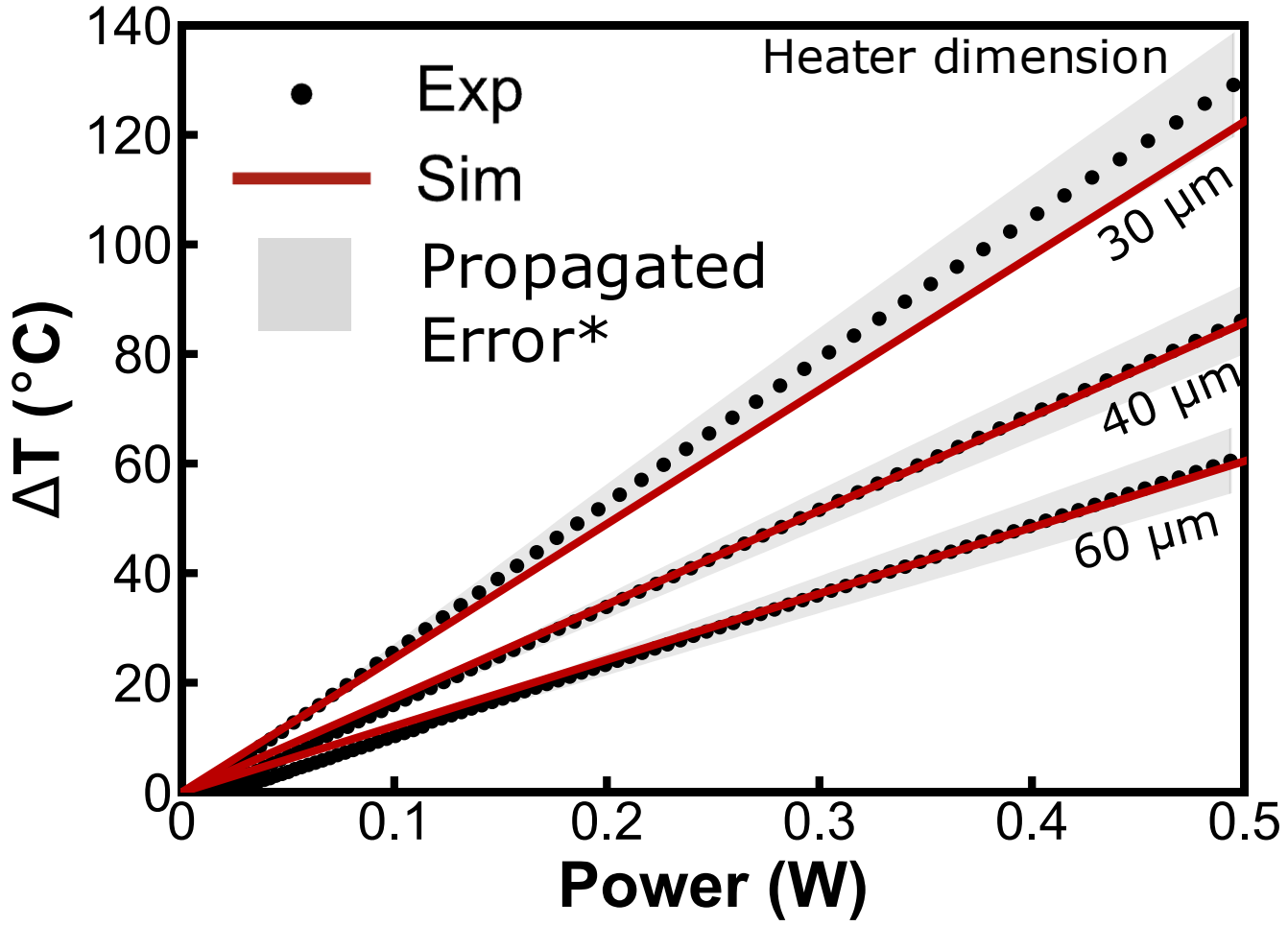
Large Benefits of 3D Thermal Scaffolding *In Hardware*



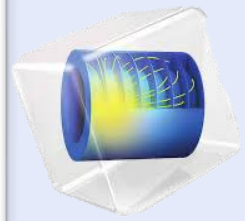


[J. Lyu IEDM 2024]

Physical Modeling of Scaffolding Experiments



COMSOL Thermal Model



All dimensions matched (e.g., diamond thickness)

Fitted parameters

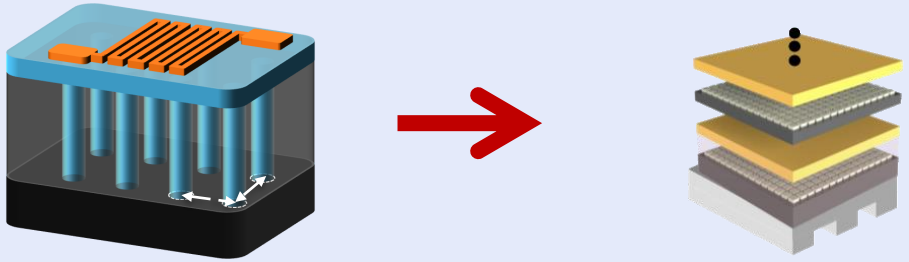
Diamond thermal conductivity	*Matches literature*
Heater thermal boundary resistance	*Not measured in literature*
External heat transfer coefficient	

[J. Lyu IEDM 2024]

**propagated through measurement and heater calibration*

Calibrated Ultra-Dense 3D Simulations

Minimal Model Changes

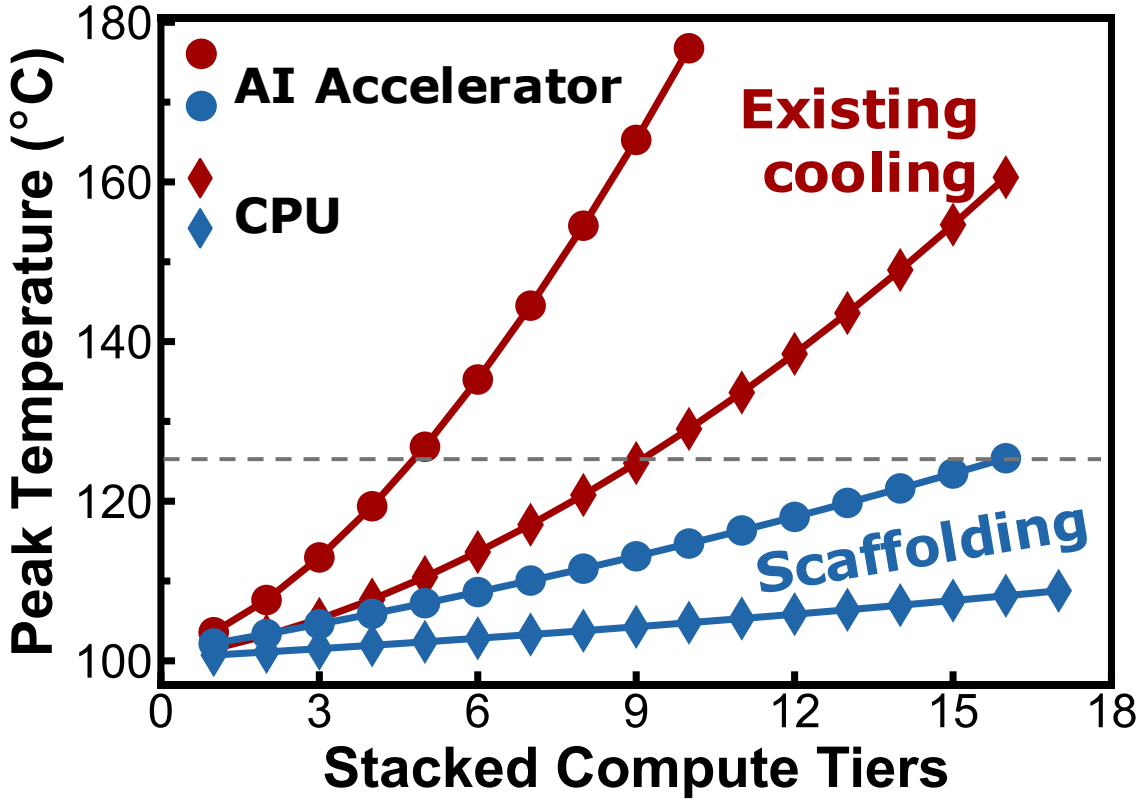


Experiment	Ultra-Dense 3D
Platform dimensions	7nm node dimensions
Heater TBR	Device TBR
Cold plate heatsink	Two-phase heatsink
Diamond vias	Copper vias
Wire heater	AI accelerator power

Large Benefits Observed

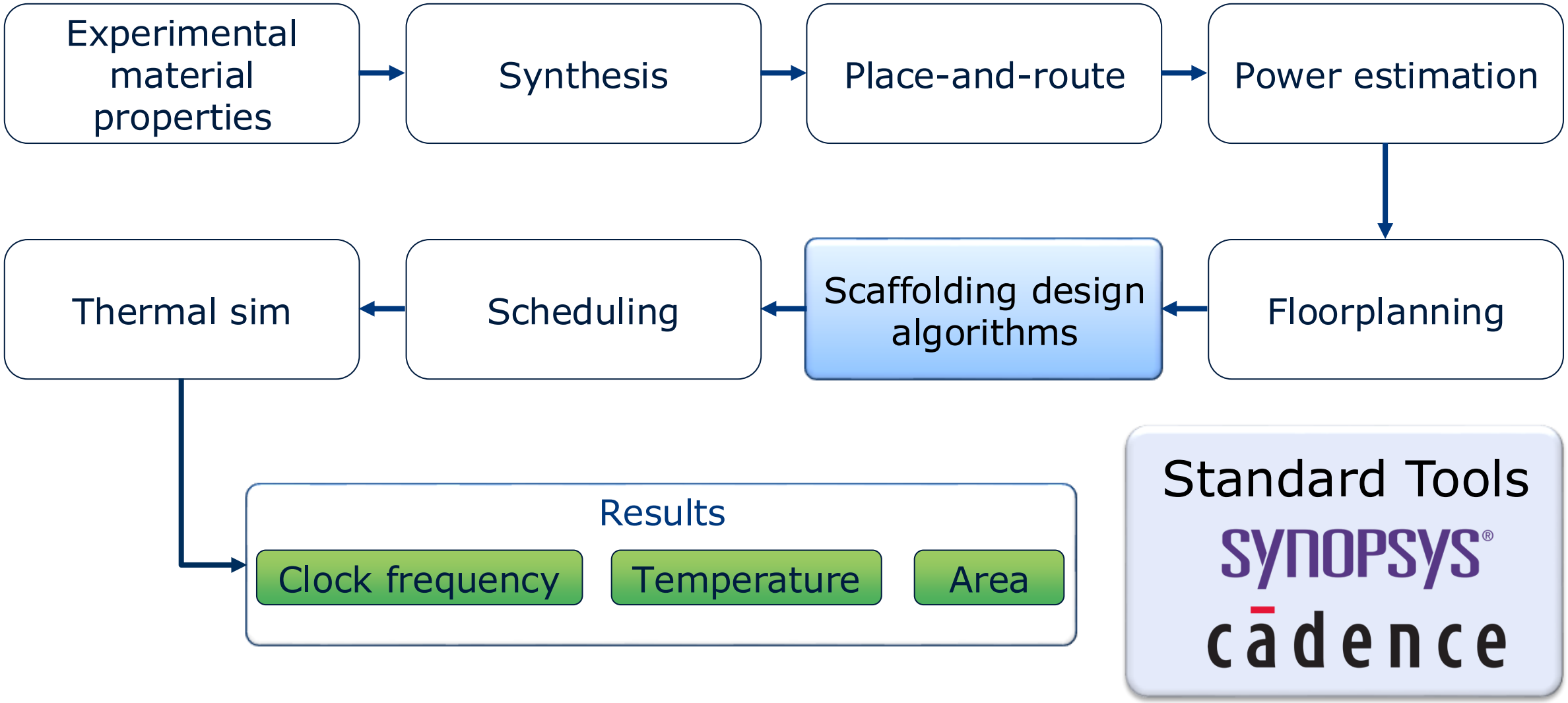
10× ΔT reduction

4× more tiers

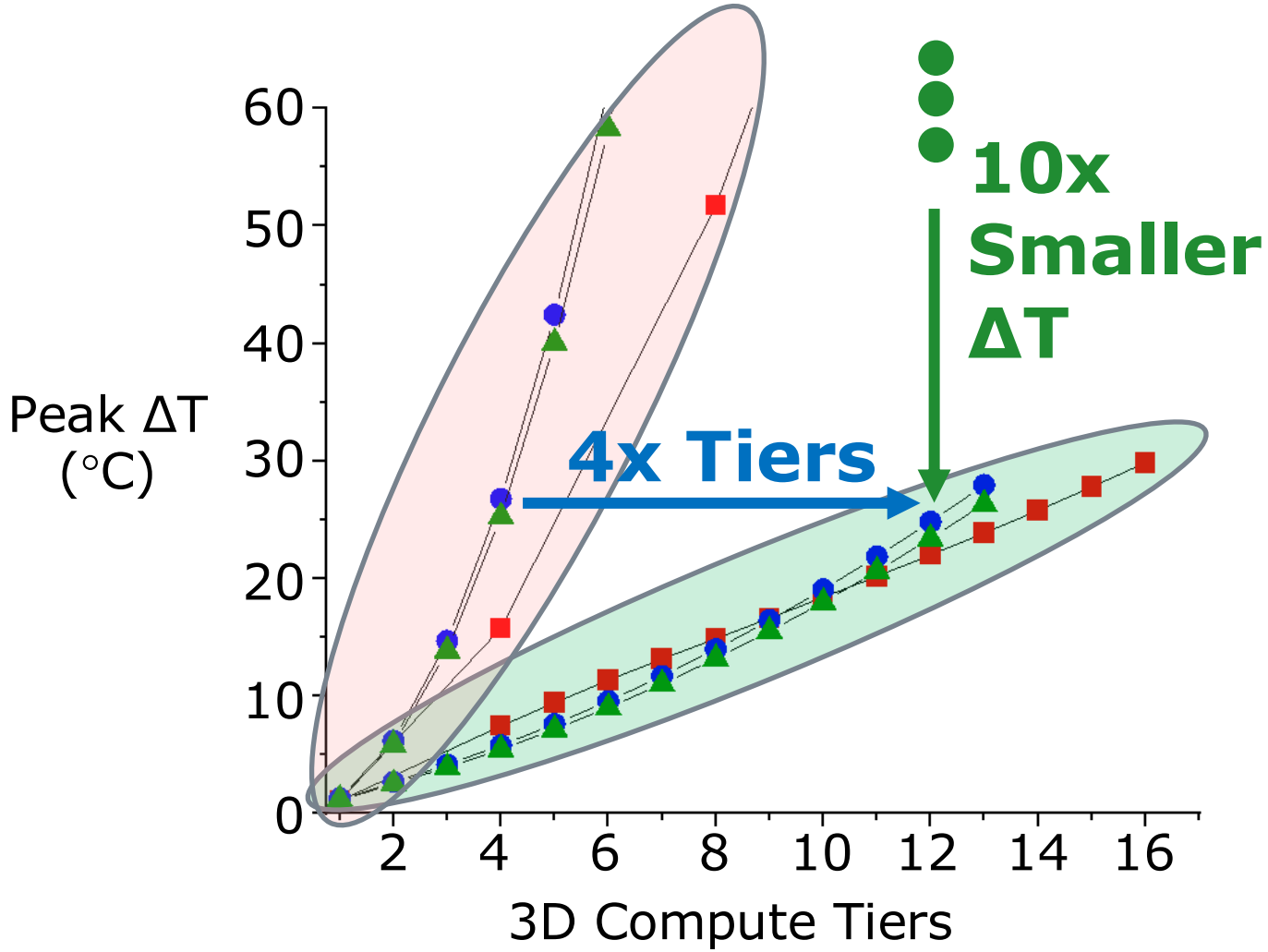


[J. Lyu IEDM 2024] TBR = Thermal Boundary Resistance

Physical Design and Modeling of Chips With Scaffolding



Benefits on Multiple Designs

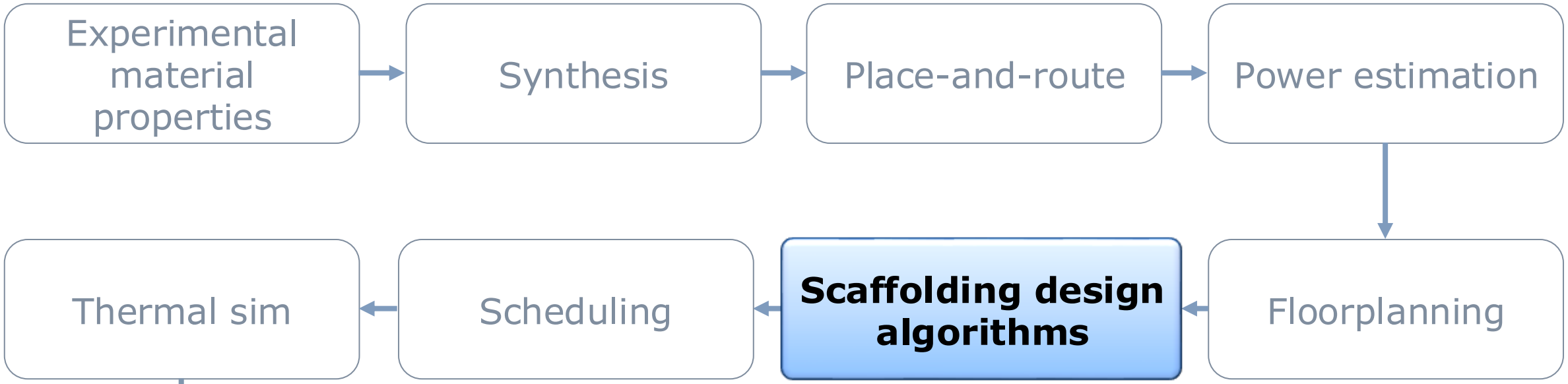


Design Requirements

Metric	Maximum Allowed
Area	1.1× Baseline
Peak Temp	125 ℃
Clock Period	1.1× Baseline
Via Pitch	100 nm*

**Peak ΔT = $T_{peak} - T_{ambient}$*Ultra-dense*

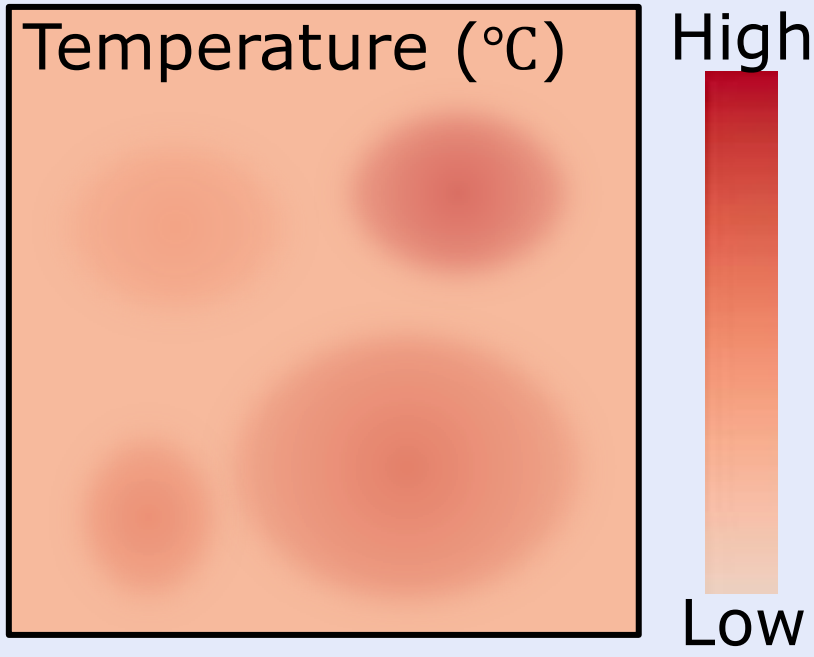
Physical Design and Modeling of Chips With Scaffolding



Place the vias and dielectric to achieve ***effective cooling*** at ***low area***

3D Thermal Scaffolding Optimization

Temperature simulation

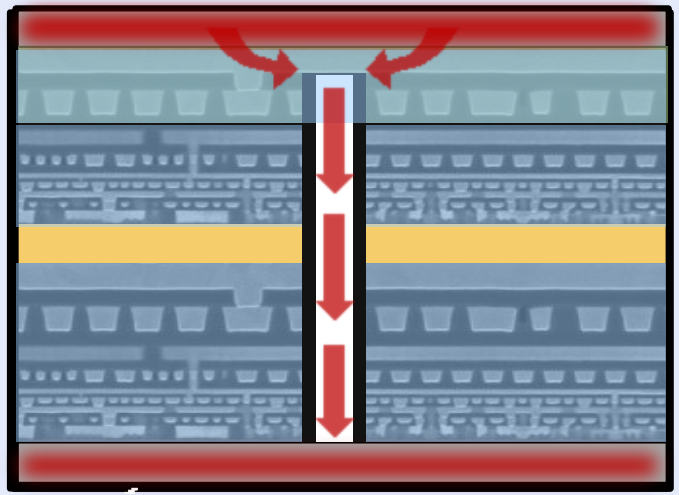


Top view

Optimization

Loop

Thermal dielectric and via placement

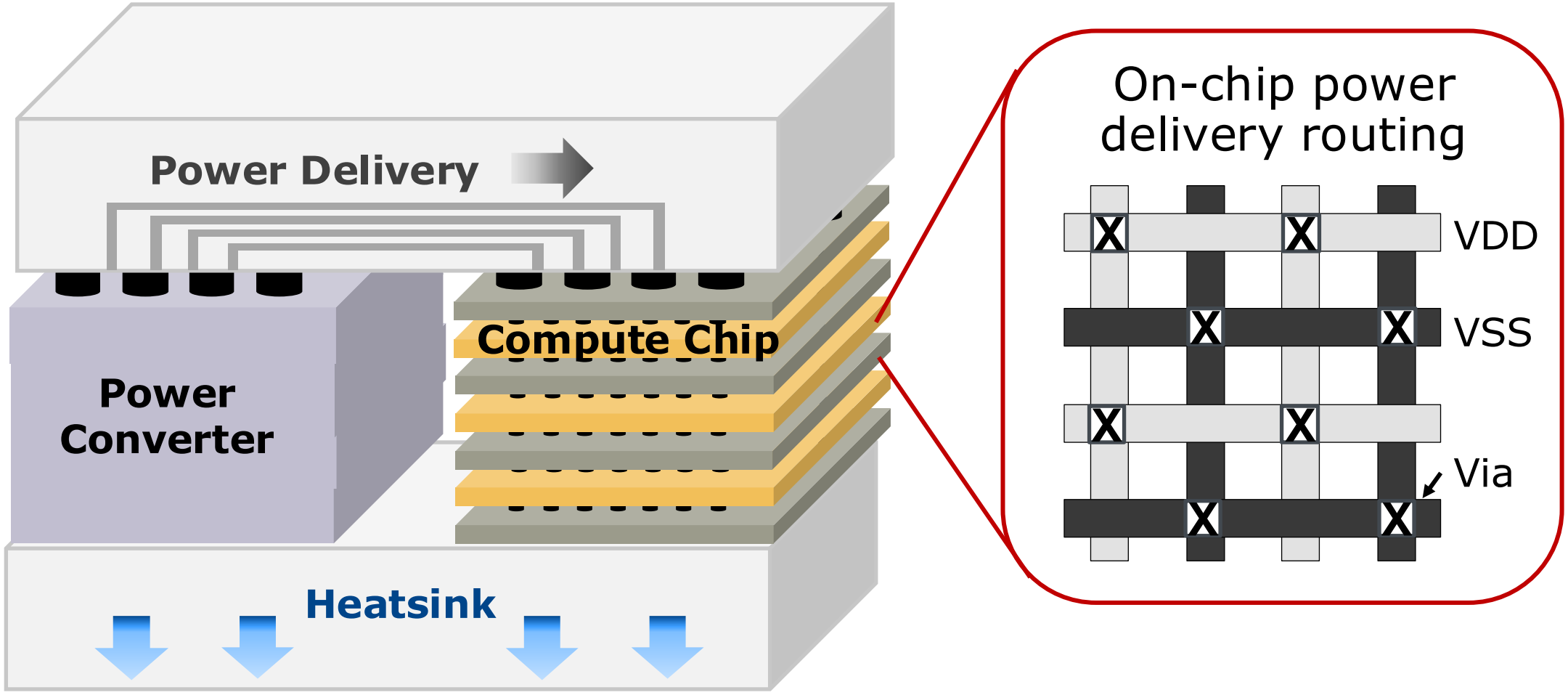


Based on simulation results

Targeting scaffolding designs to hotspots ***reduces area***

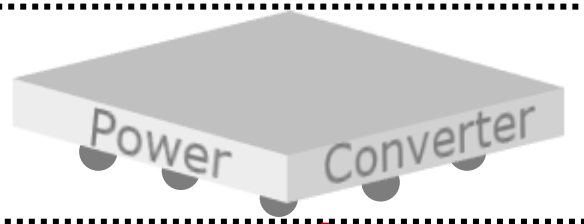
IR Drop

Minimize resistive IR drop associated with path to chip

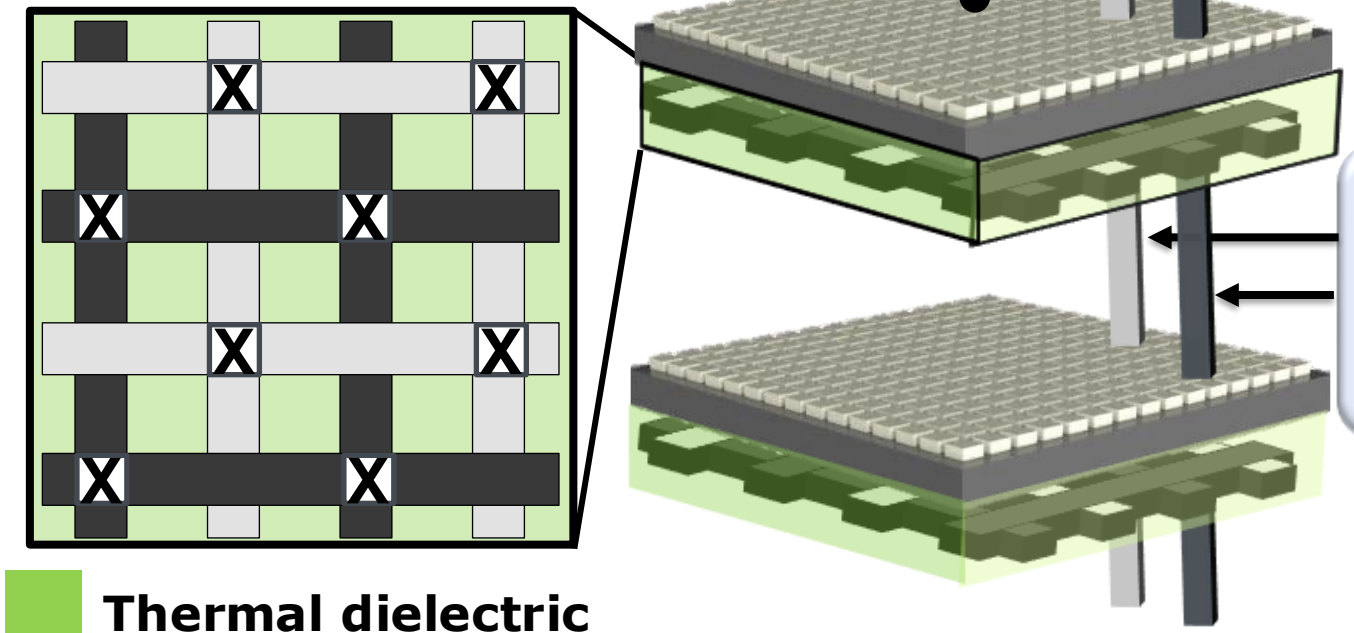


Reducing IR Drop Using 3D Thermal Scaffolding

Off-chip:
not considered today



Massive vertical current density



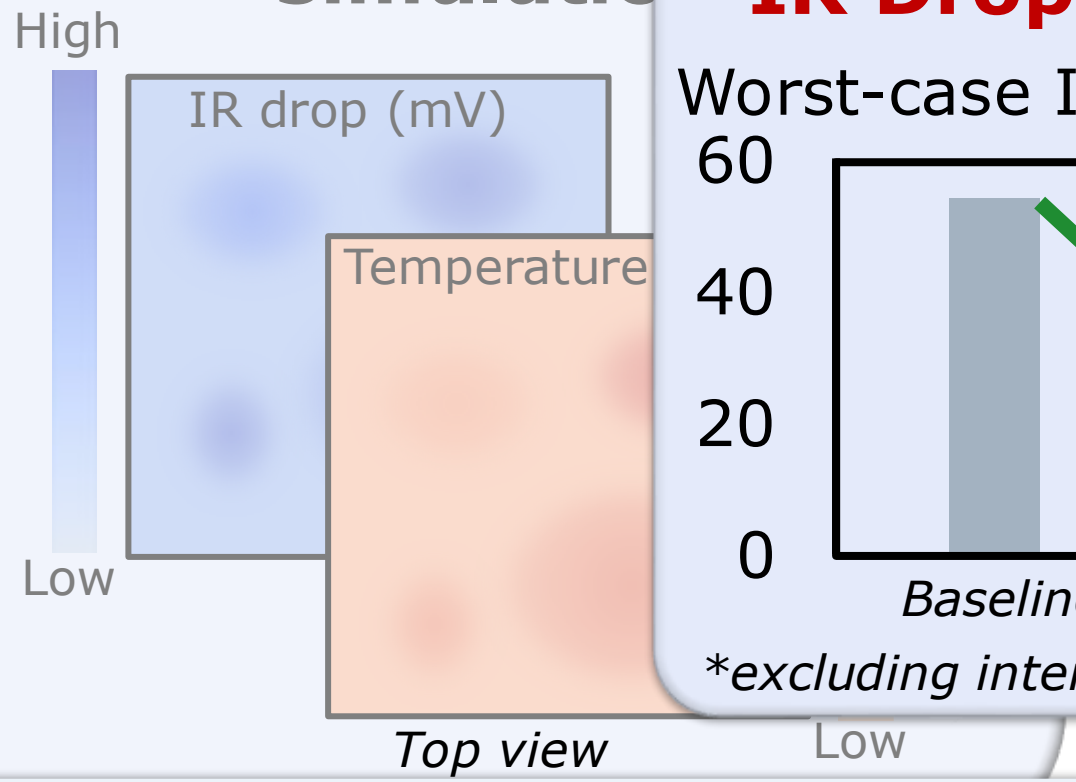
Thermal dielectric

Vias used *simultaneously* for heat and current

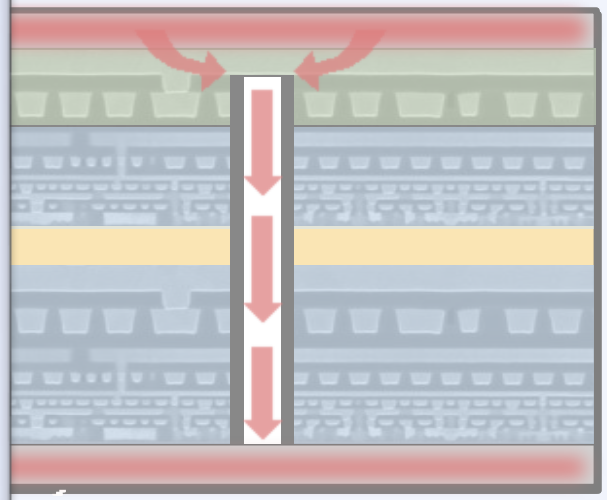
To heatsink

3D Thermal Scaffolding Optimization

IR drop and **temperature** simulatio



Thermal dielectric and **ia placement**



Based on simulation results

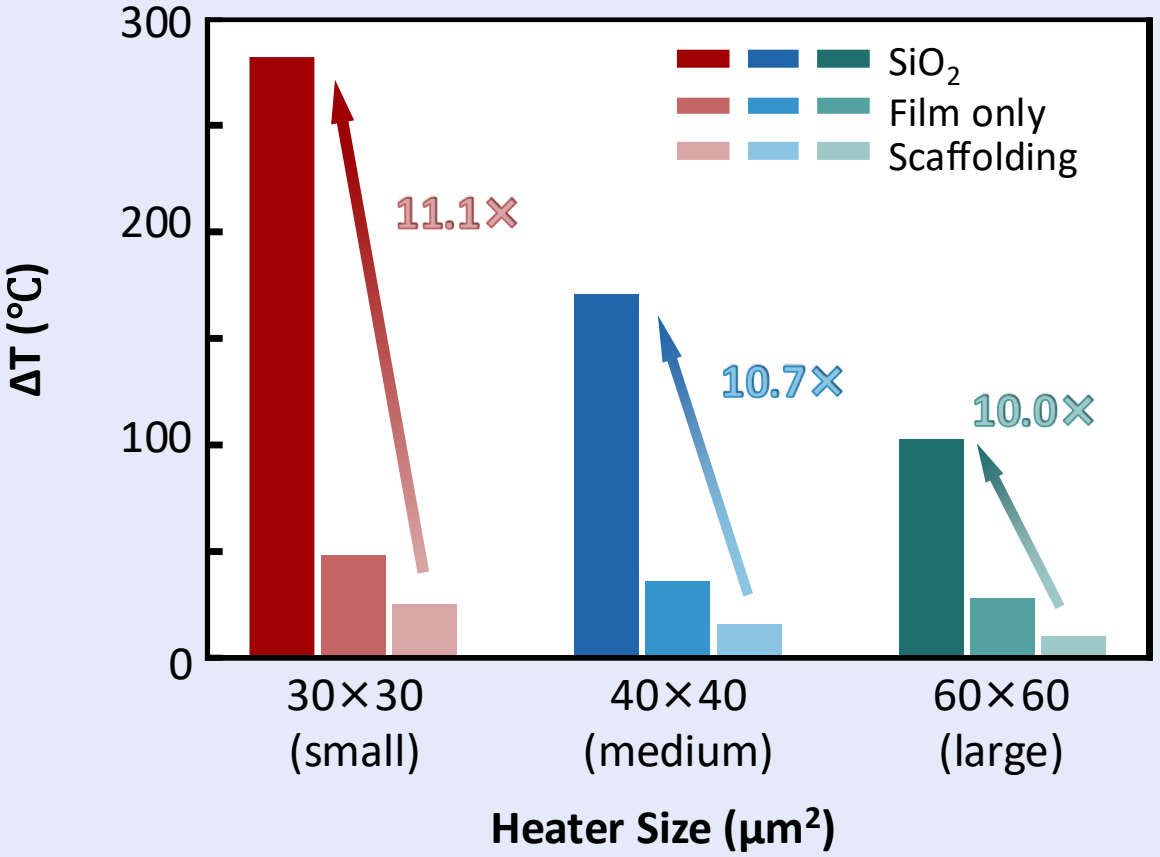
IR Drop Benefits

**excluding interposer, converter*

Simultaneous cooling and IR drop at same area penalty

3D Thermal Scaffolding

Consistent >10× Cooling
Across Heater Sizes



All heaters at 0.1W

Calibrated Simulations
Large Benefits Validated

AI accelerator layers in 3D (T_{peak} = 124°C)	**4×** more (12 vs. 3)
Peak ΔT (12 AI accelerator layers in 3D)	**10×** lower (24°C vs. 251°C)
Area penalty (12 AI accelerator layers in 3D)	**14×** less (5.5% vs. 78%)

$$\text{Peak } \Delta T = T_{peak} - T_{ambient}$$

[J. Lyu IEDM 2024] Collaborator: Prof. S. Chowdhury (Stanford)