Dipole Engineering for Tunable Retention in Gain Cell Memory

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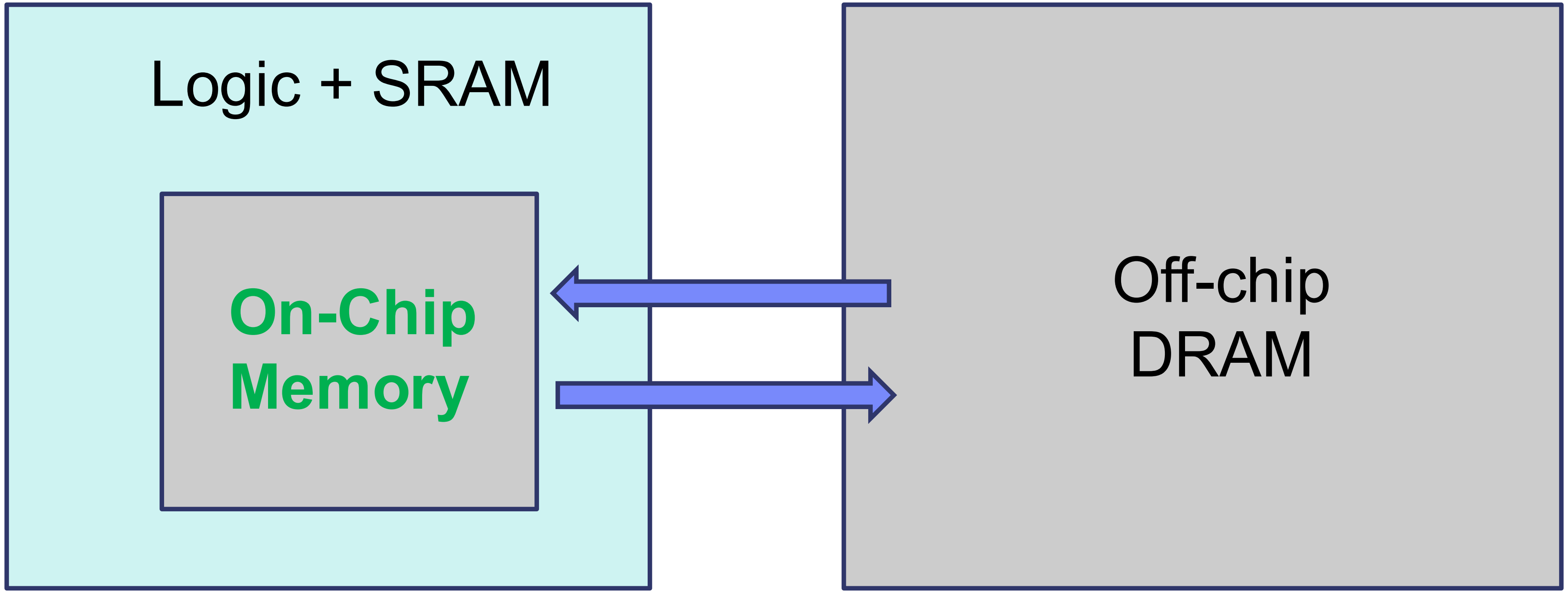
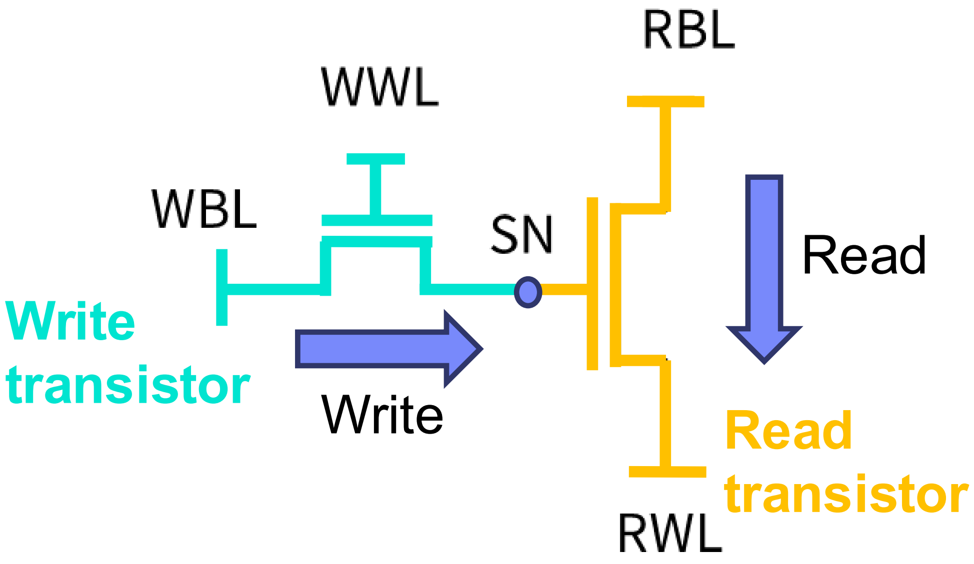
On-Chip Memory



- **High bandwidth on-chip memory can be a solution**

- *M. Aly, …, H.-S. P. Wong, S. Mitra, Computer, 2015*
- *M. Aly, … H.-S. P. Wong, S. Mitra, Proc. IEEE, 2019*

2T Gain Cell



WWL : Write wordline
WBL : Write bitline
RWL : Read wordline
RBL : Read bitline
SN : Storage node

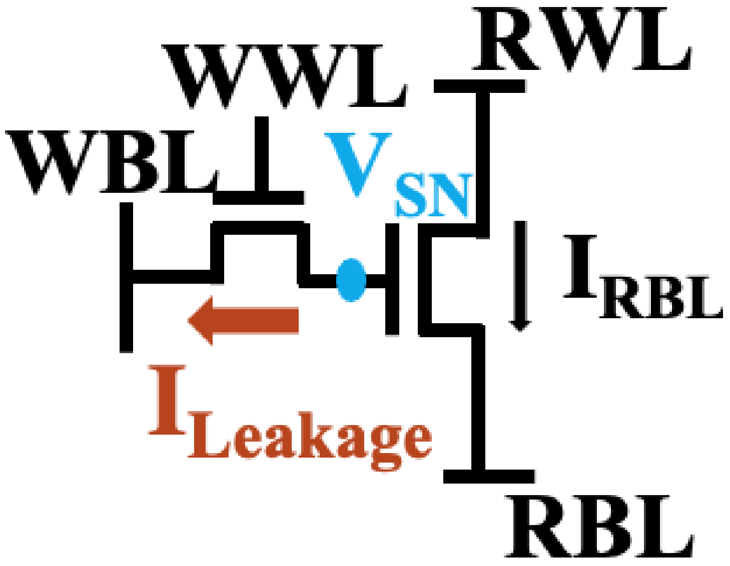
- ✓ **Logic compatible**
- ✓ **Nondestructive read**
- ✓ **Amplify Stored Charge by a read transistor**
- ✓ **Denser than SRAM**

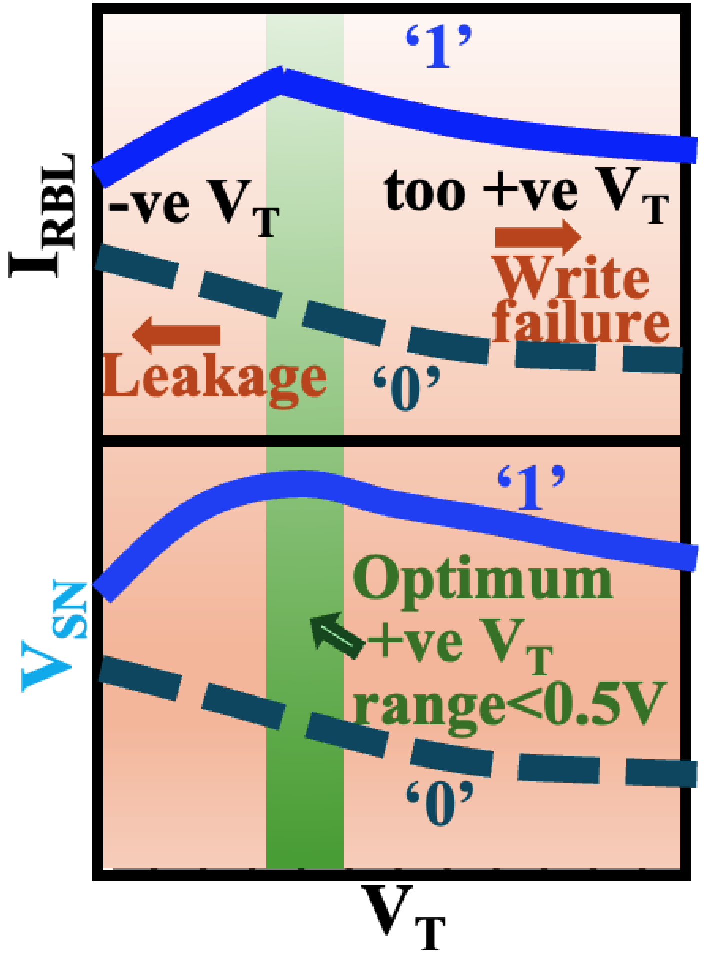
*2T: Two Transistors

Precise control of V_T is essential in Gain Cell

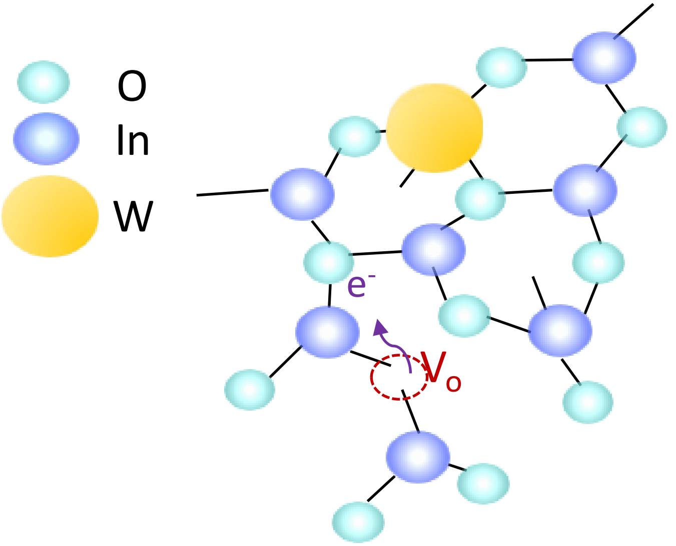
- Negative V_T leads to retention failure due to leakage
- Excessively positive V_T results in write failure

2T Gain Cell



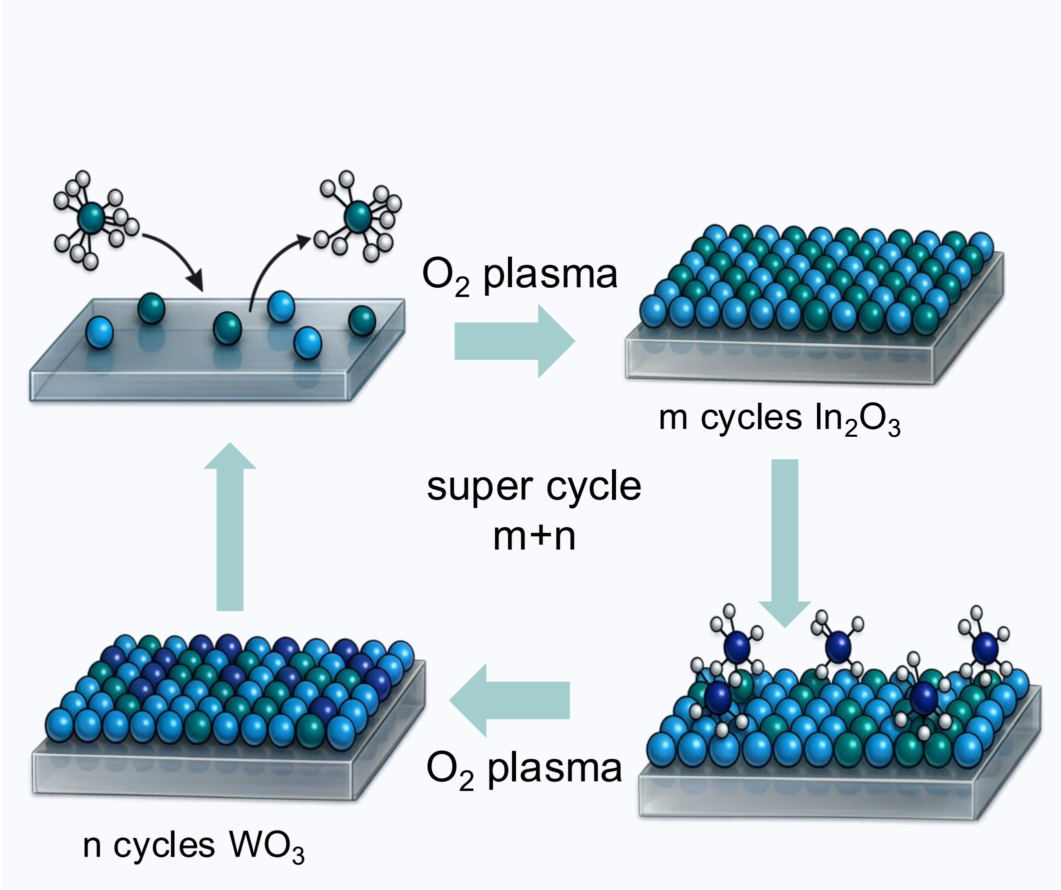


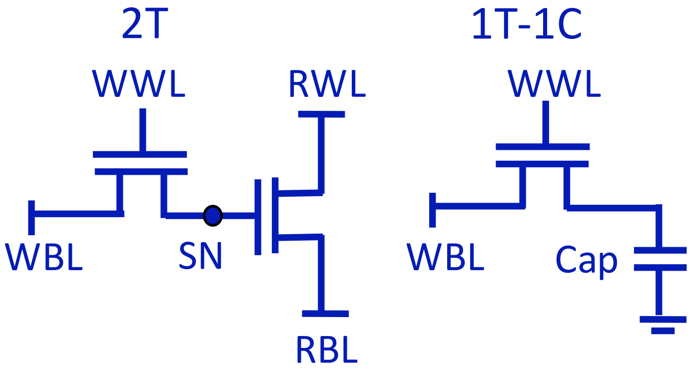
BEOL Compatible Amorphous Oxide Semiconductors (AOS)

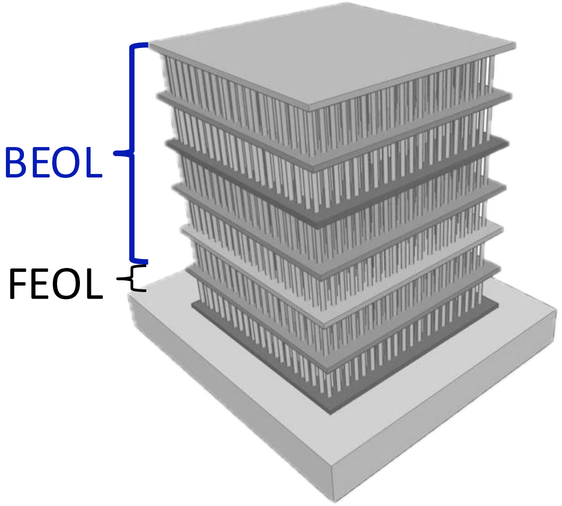


e.g., ITO, IO, IWO, IGZO

Plasma Enhanced Atomic Layer Deposition (ALD)



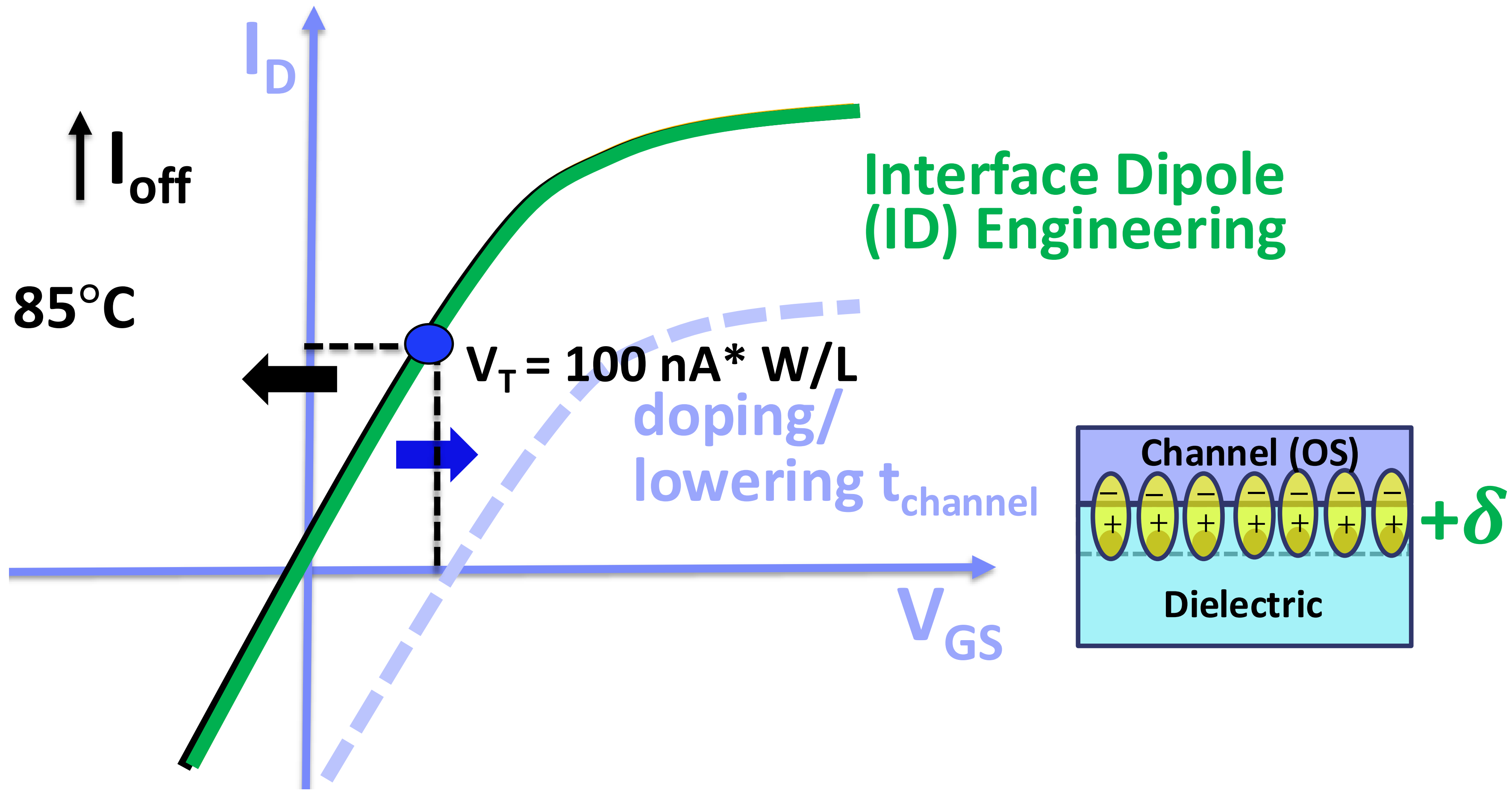




FEOL: front end of line, BEOL: back end of line, 2T: two transistor, 1T-1C: two transistor one capacitor

Precise control of V_T is Difficult in Oxide Semiconductor FET

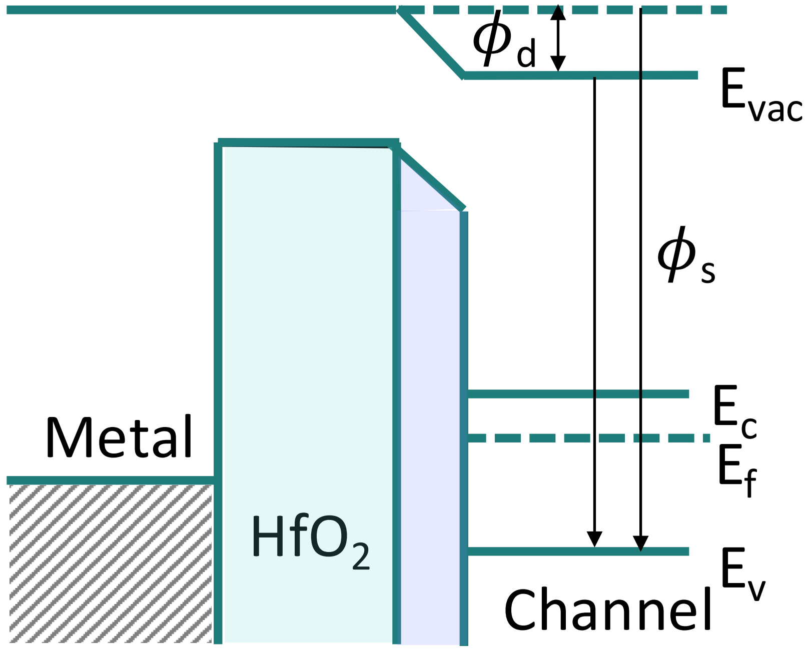
- ID engineering should shift V_T without affecting other device properties (e.g., mobility, I_{on}, SS)



SS: subthreshold swing

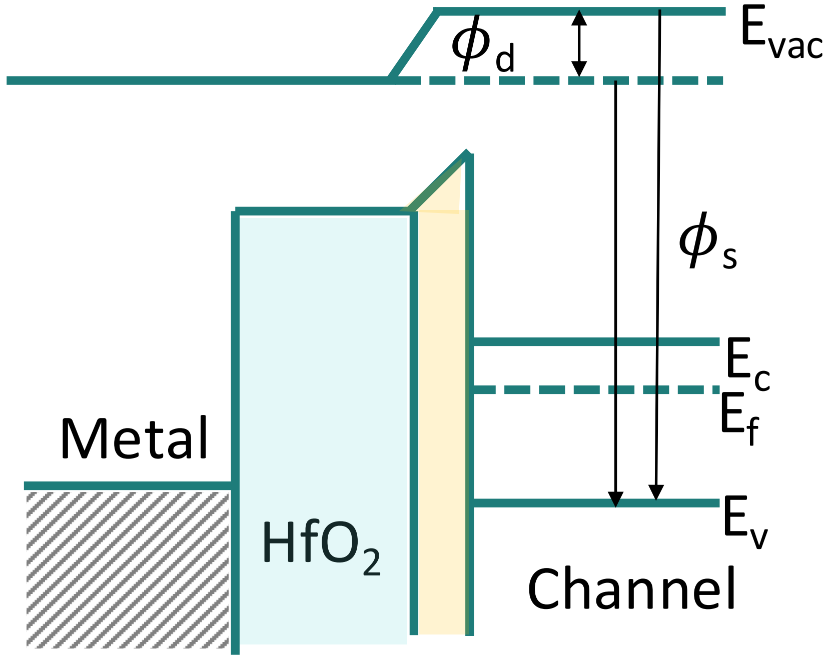
Negative and Positive Interfacial Dipole

$V_T = V_{T0} - \Delta V_{dip}$



Negative dipole

$V_T = V_{T0} + \Delta V_{dip}$



Positive dipole

🟦 Negative dipole layer

🟨 Positive dipole layer

Dipole Engineered OSFETs Fabrication

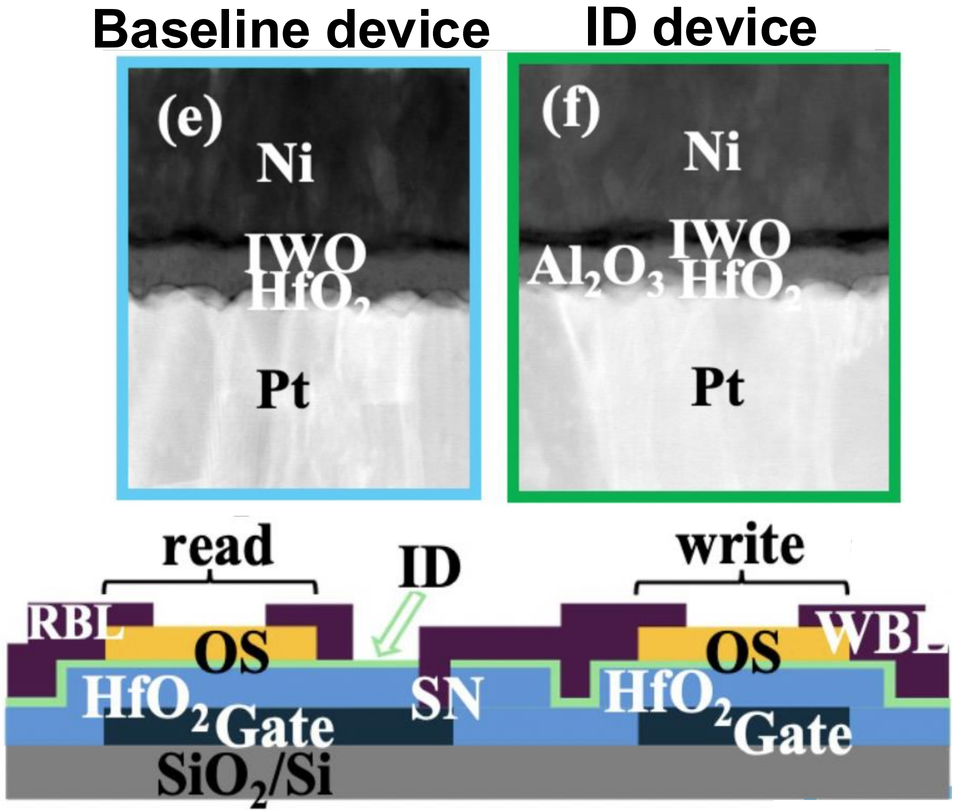
- Gate: e-beam Ti/Pt (5 nm /70 nm)
- Dielectric: ALD HfO_2; O_2 plasma @ 200°C
- ID forming layer: ALD Al_2O_3 O_2 plasma @ 200 °C, (1) 0.2 nm, (2) 0.6 nm, (3) 0.9 nm
- Channel: ALD IWO, 3 nm, O_2 plasma @ 225°C
- S/D: e-beam evaporation Ni/Au(50 nm/50 nm)

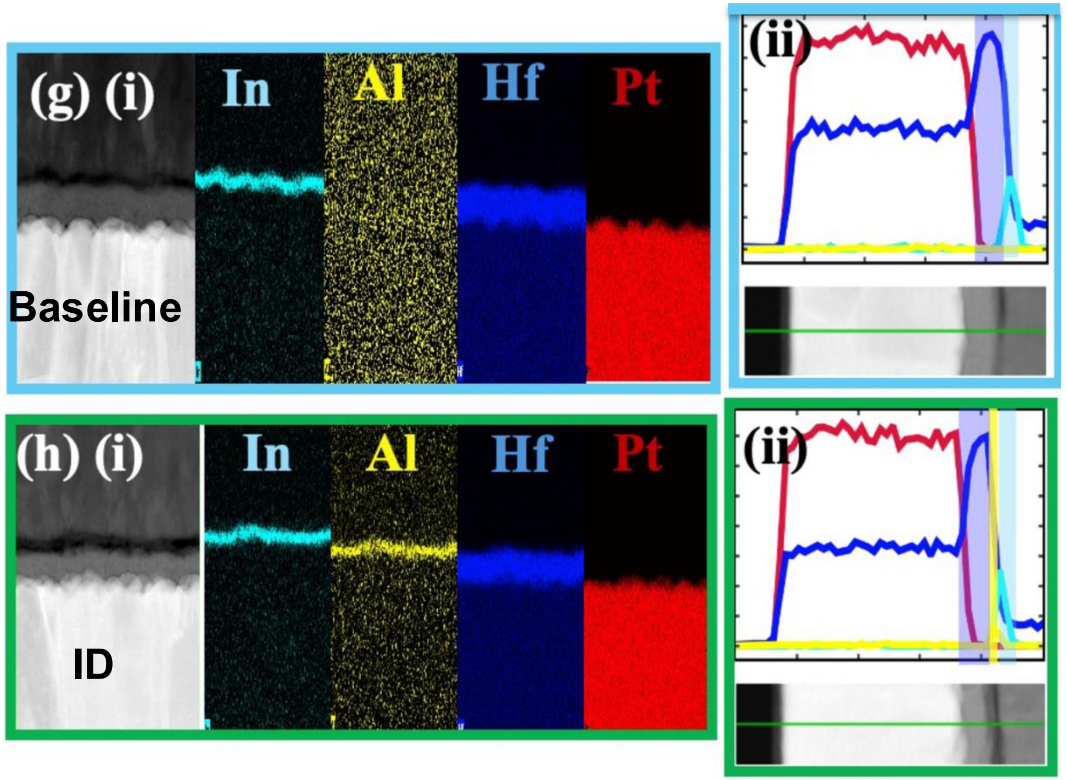
**max. process temp. < 225°C

ALD: atomic layer deposition, OSFET: oxide semiconductor field effect transistor

Thin Alumina at OS/Dielectric Interface

- TEM and EDS images reveal a thin Al_2O_3 layer in between the dielectric and oxide semiconductor (OS) channel in the ID (Interface dipole) device



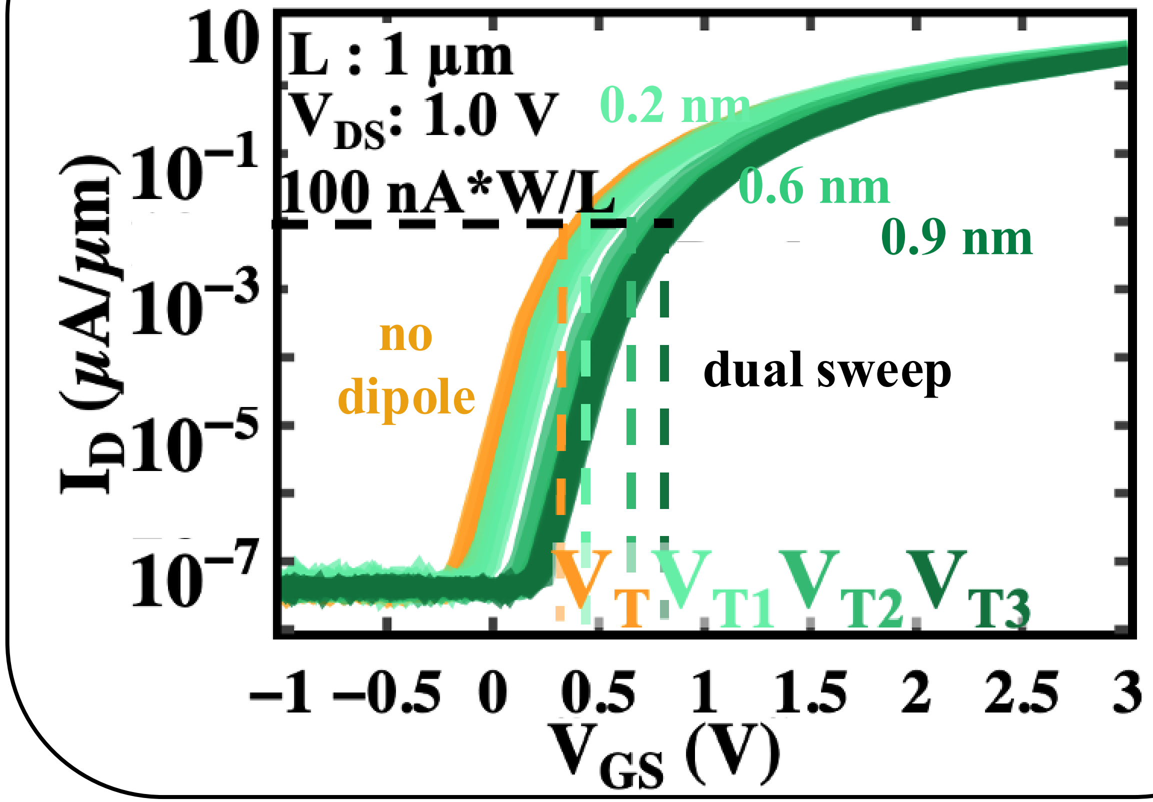


TEM: transmission electron microscopy, EDS: electron dispersion microscopy

Multi V_T can be achieved

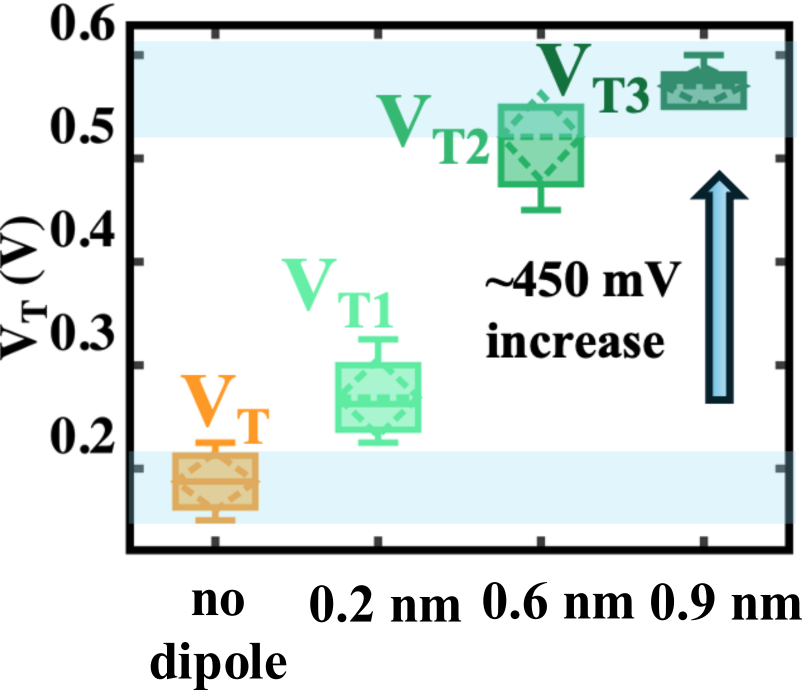
- Multiple V_T can be achieved with a maximum increase of ~450-500 mV from STD

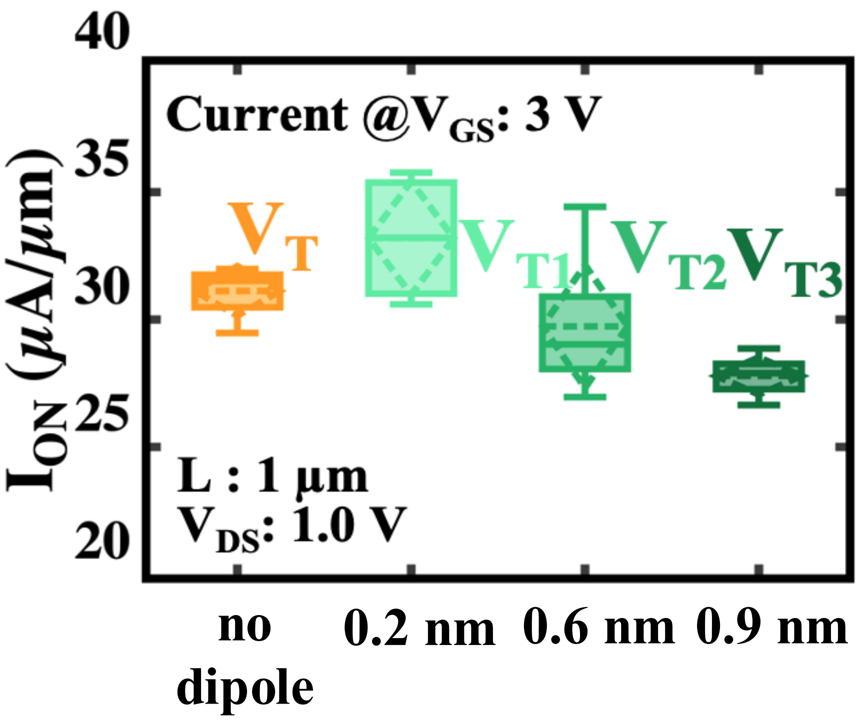
Dipole engineering for Oxide Semiconductors

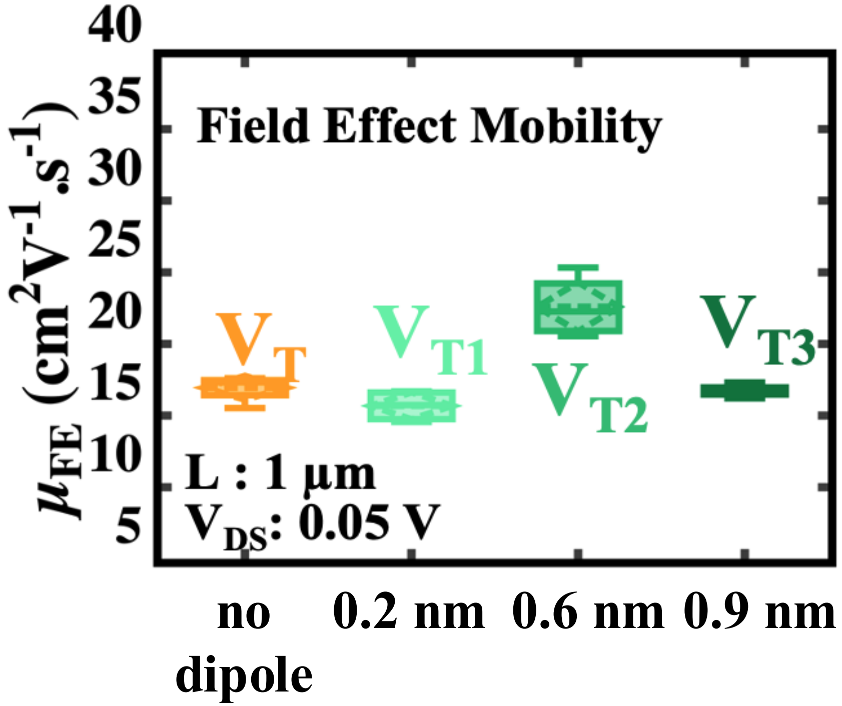


Dipole is an ‘*Orthogonal*’ Knob

- V_T tuning without affecting I_{on} @ V_{GS} = 3 V and μ_{FE}



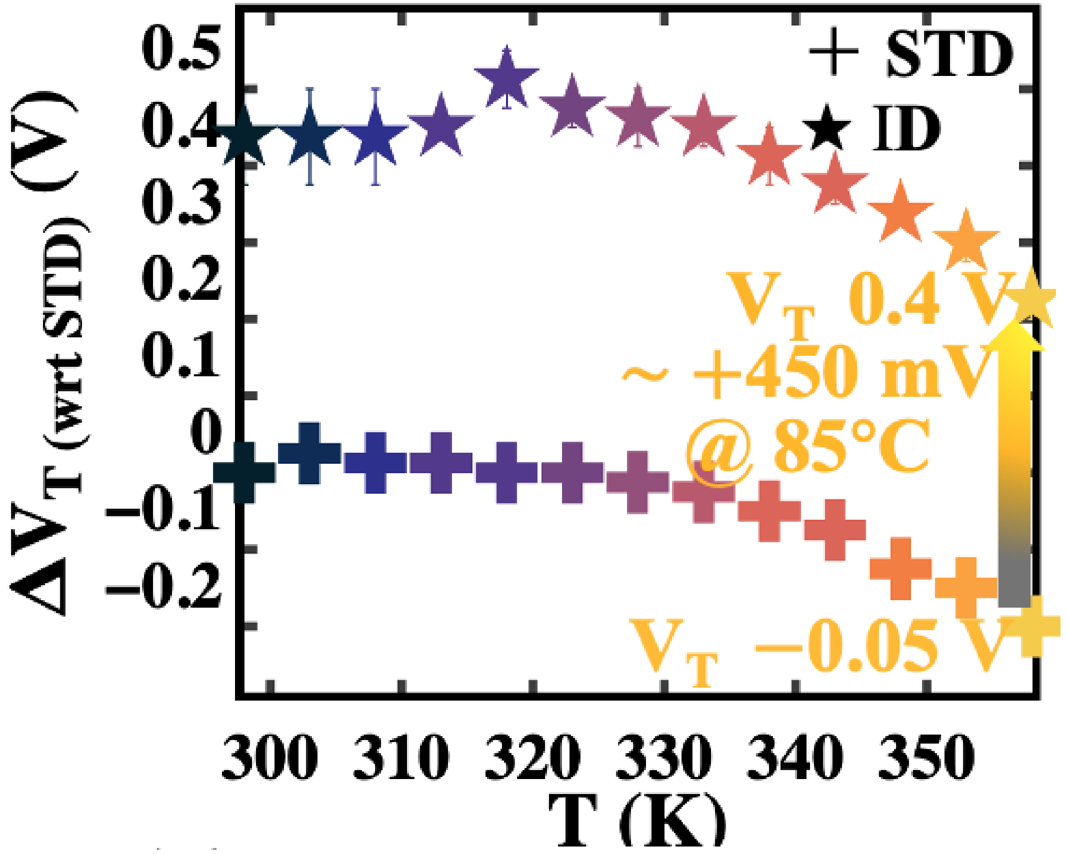


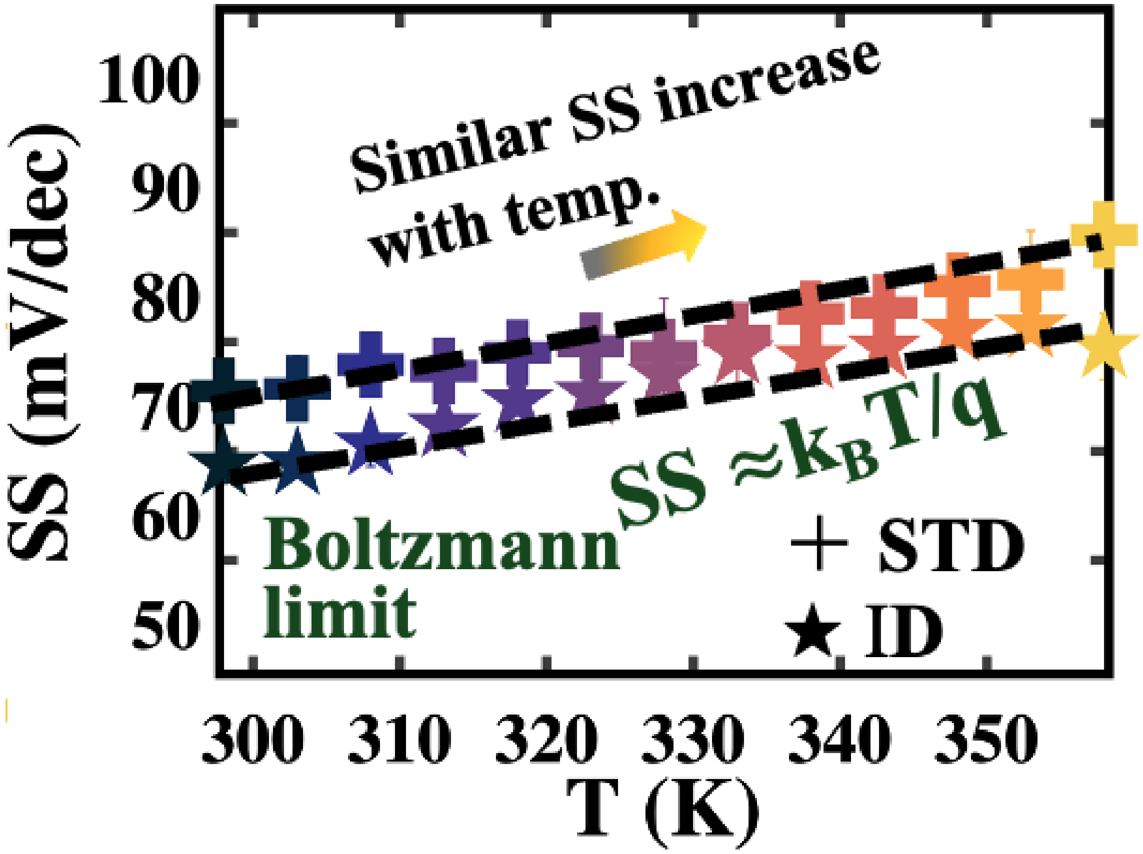


μ_{FE}: field effect mobility

High Temperature V_T

- V_T difference from the STD device remains ~450 mV at 85°C

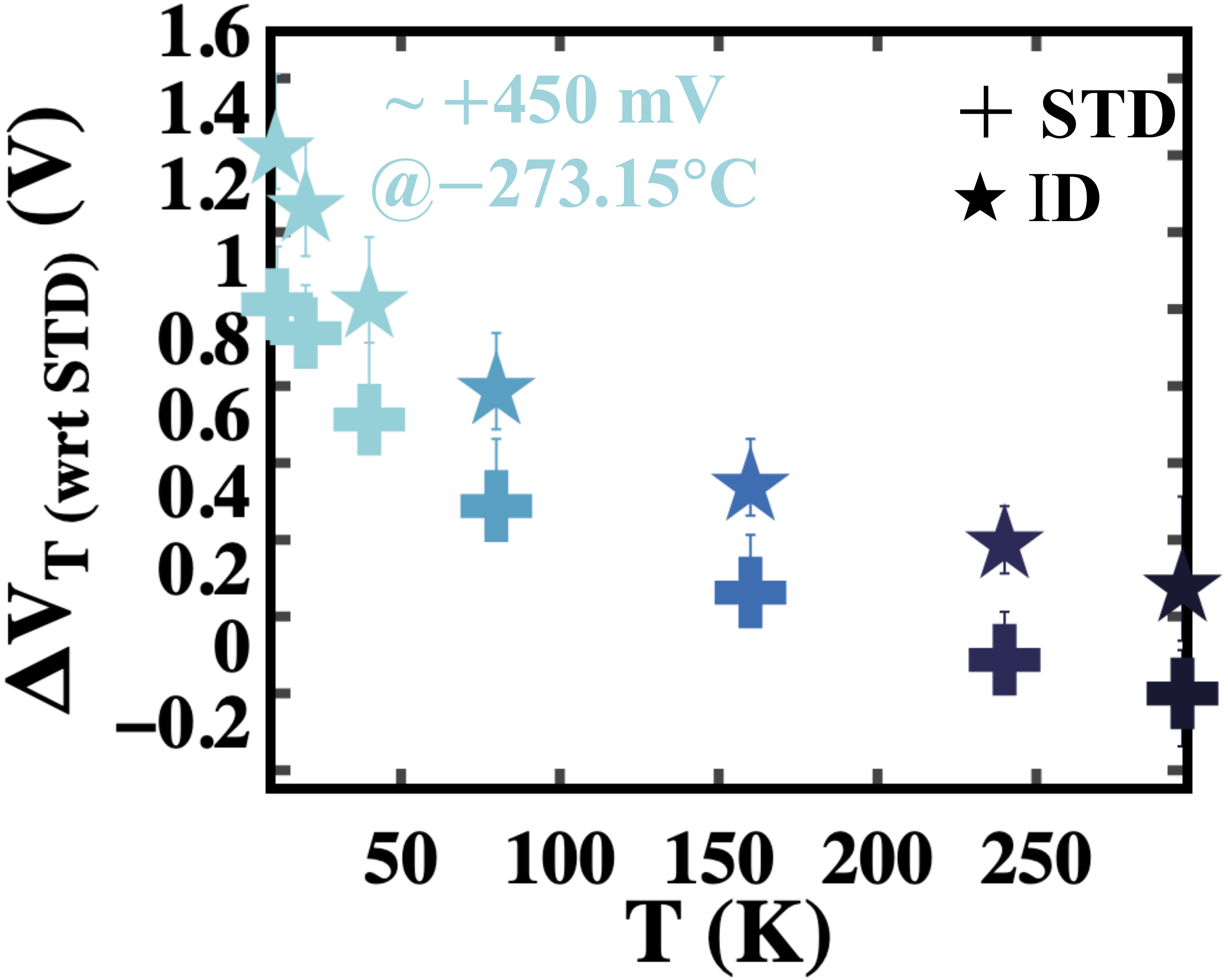




SS: subthreshold swing

Cryogenic temperature V_T

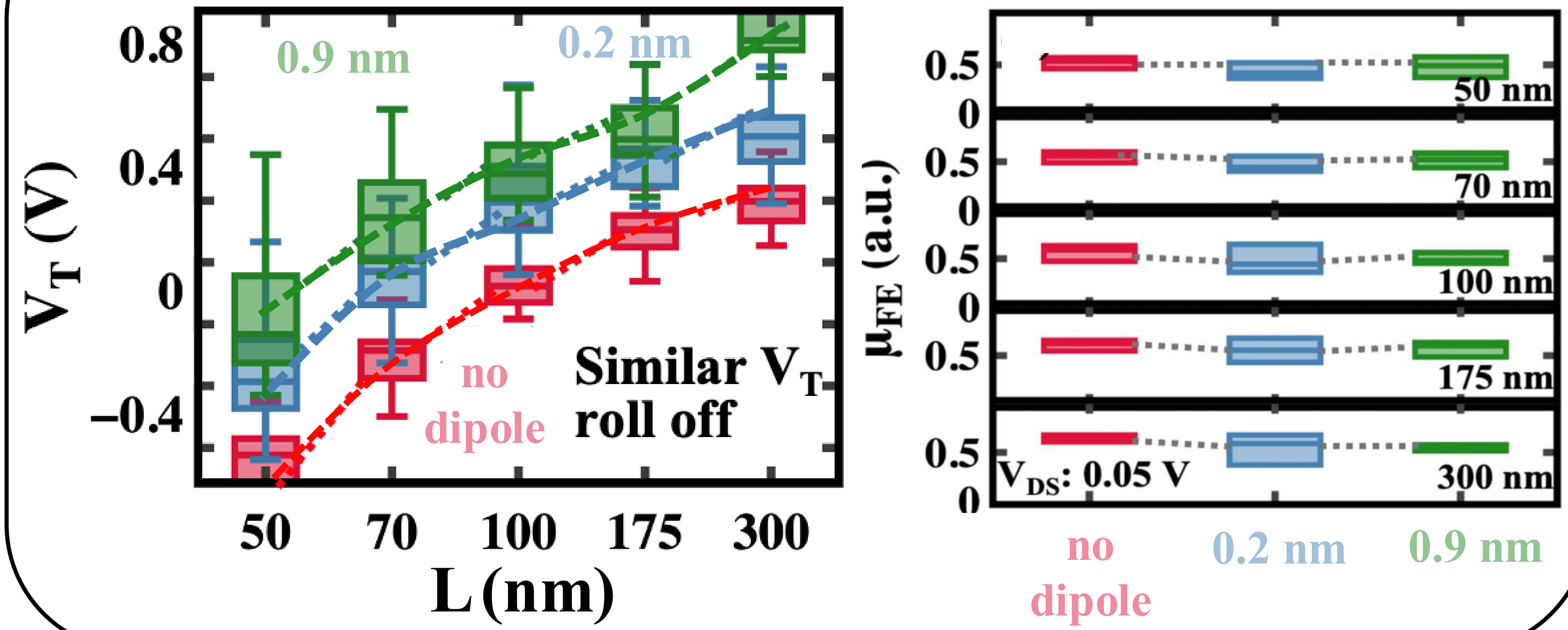
- V_T difference from the STD device remains ~450 mV at -10 K



Dipole enables comparable V_T roll off in short channel

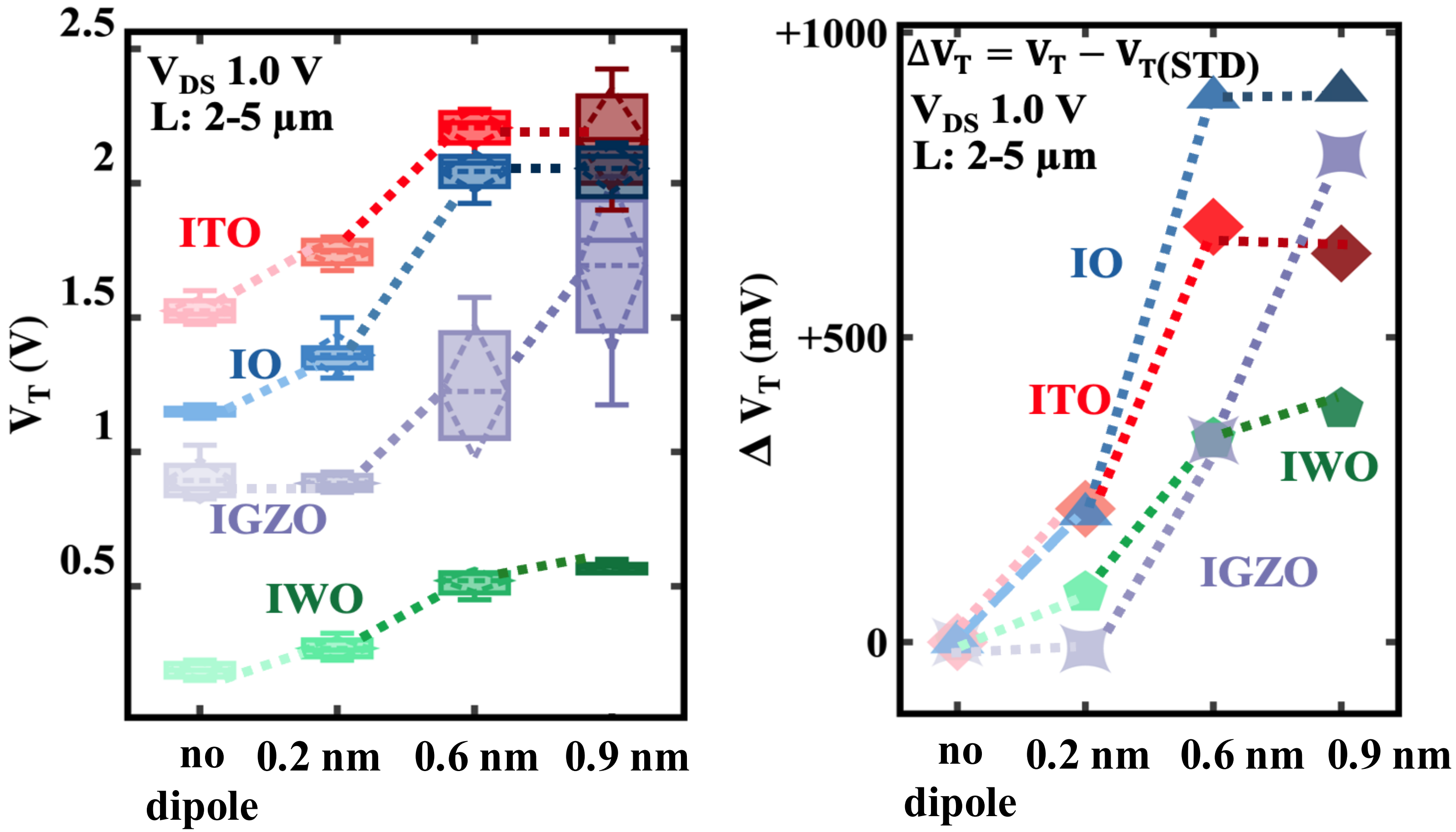
- μ_{FE} remains similar across varying channel length
- Comparable V_T roll-off

Oxide Semiconductor FETs Dipole Engineering



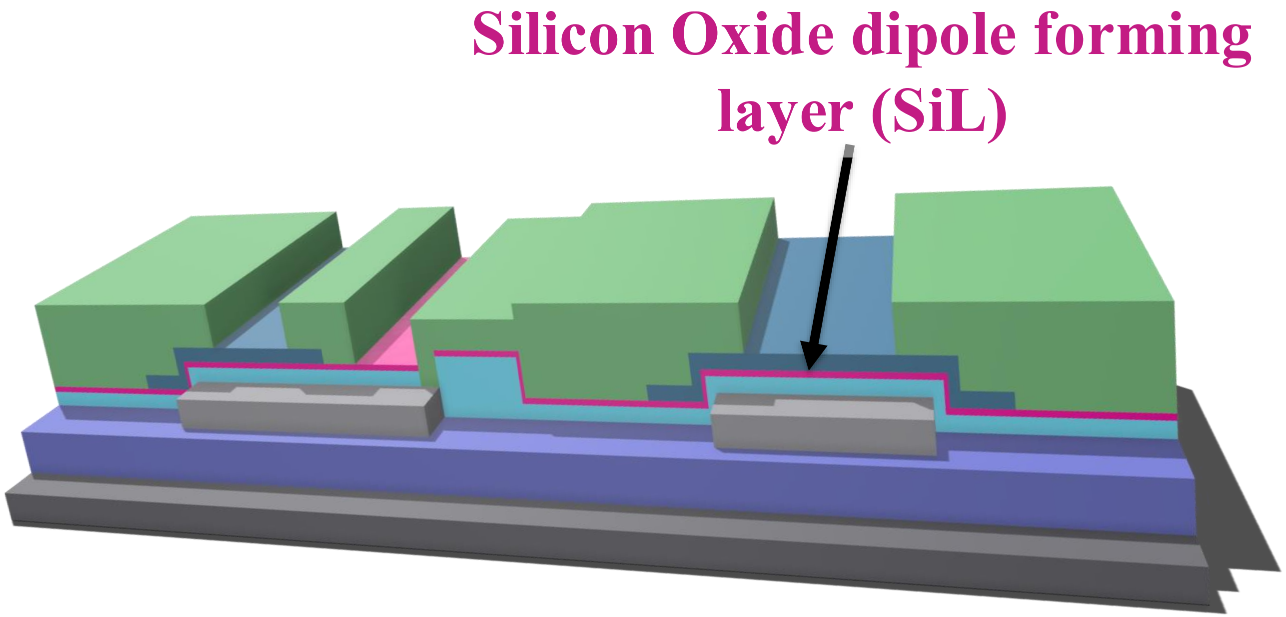
Different Oxide Semiconductors

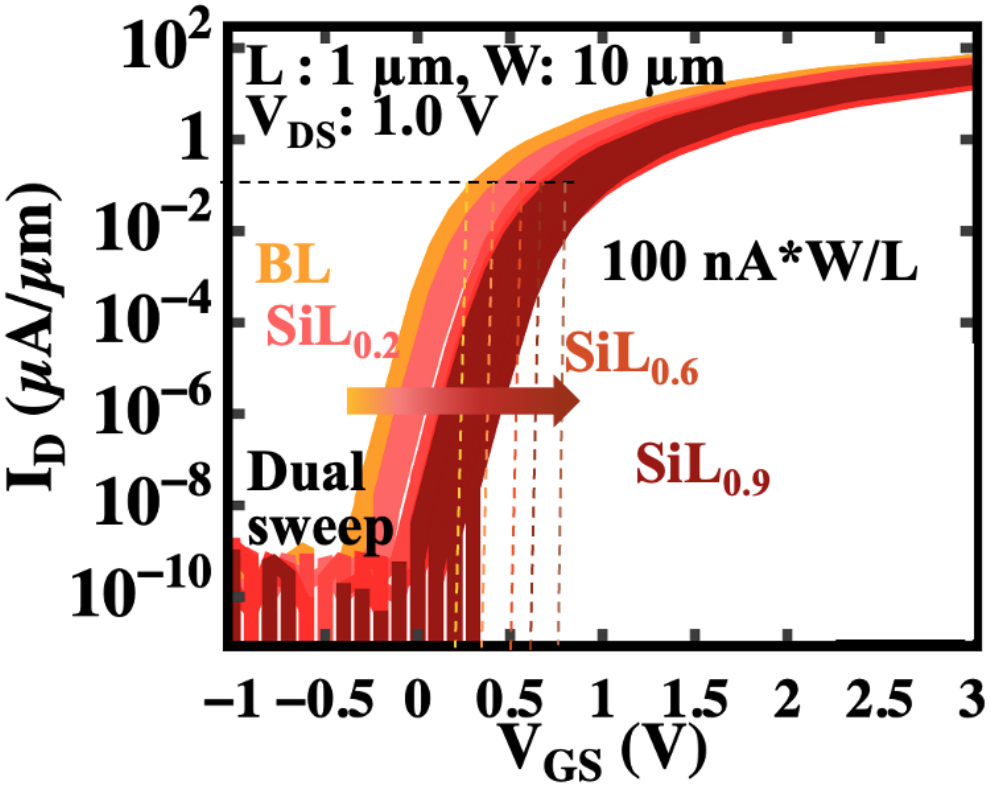
- V_T shift with dipole is possible for different oxide semiconductor materials
- SiO_x is another dipole shifter for oxide semiconductors



Another Dipole-Forming Candidate: SiO_x

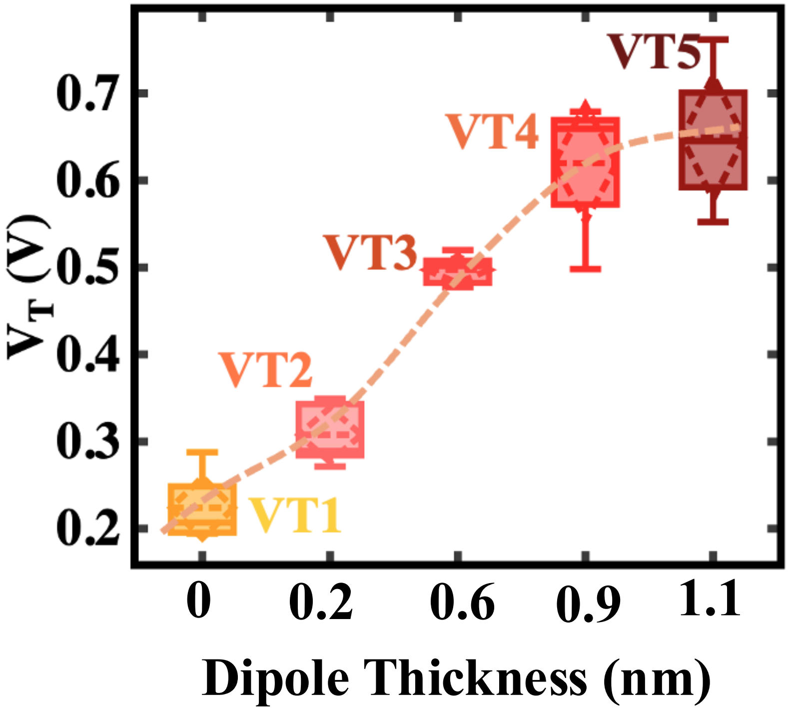
- SiO_x is another dipole shifter for oxide semiconductor FETs

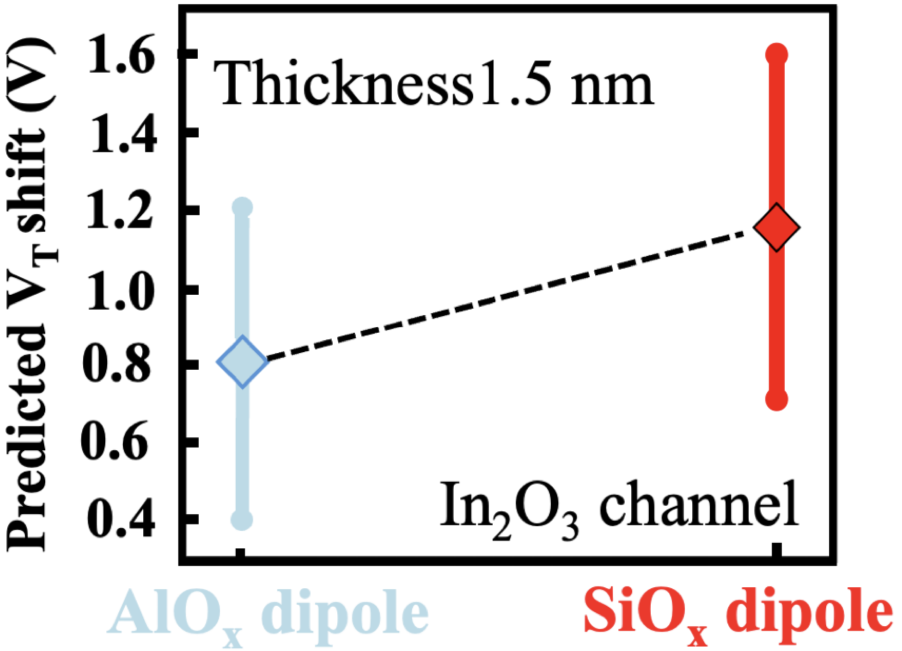


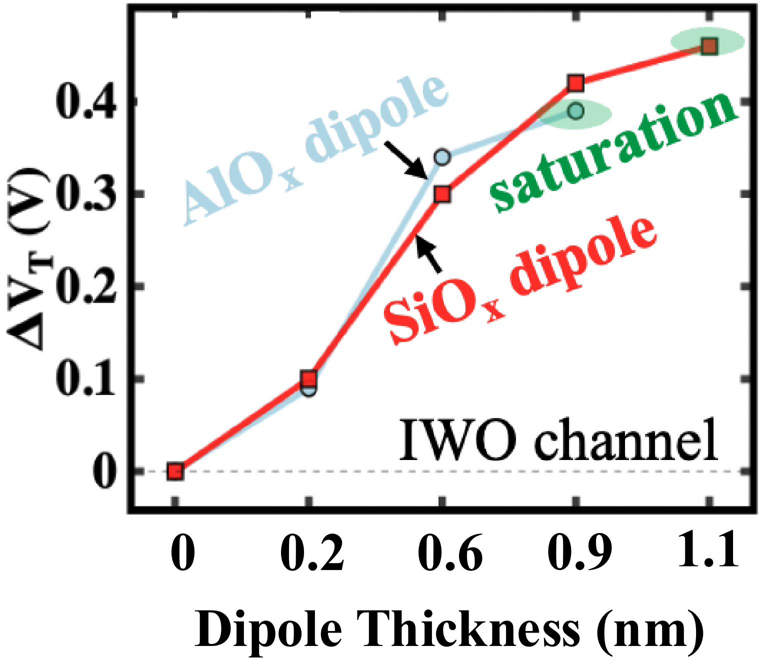


Finer V_T control with SiO_x dipole

- SiO_x dipole enables fine-grained V_T tuning
- Compared with an AlO_x dipole of the same thickness, SiO_x achieves a larger V_T shift

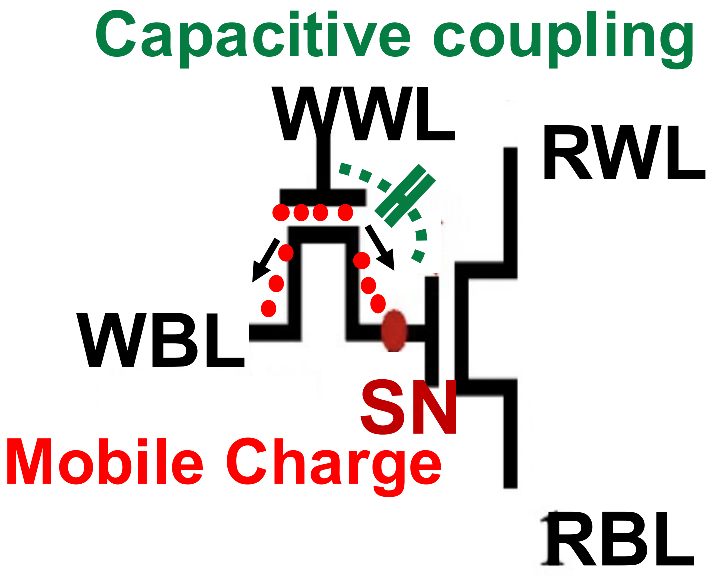


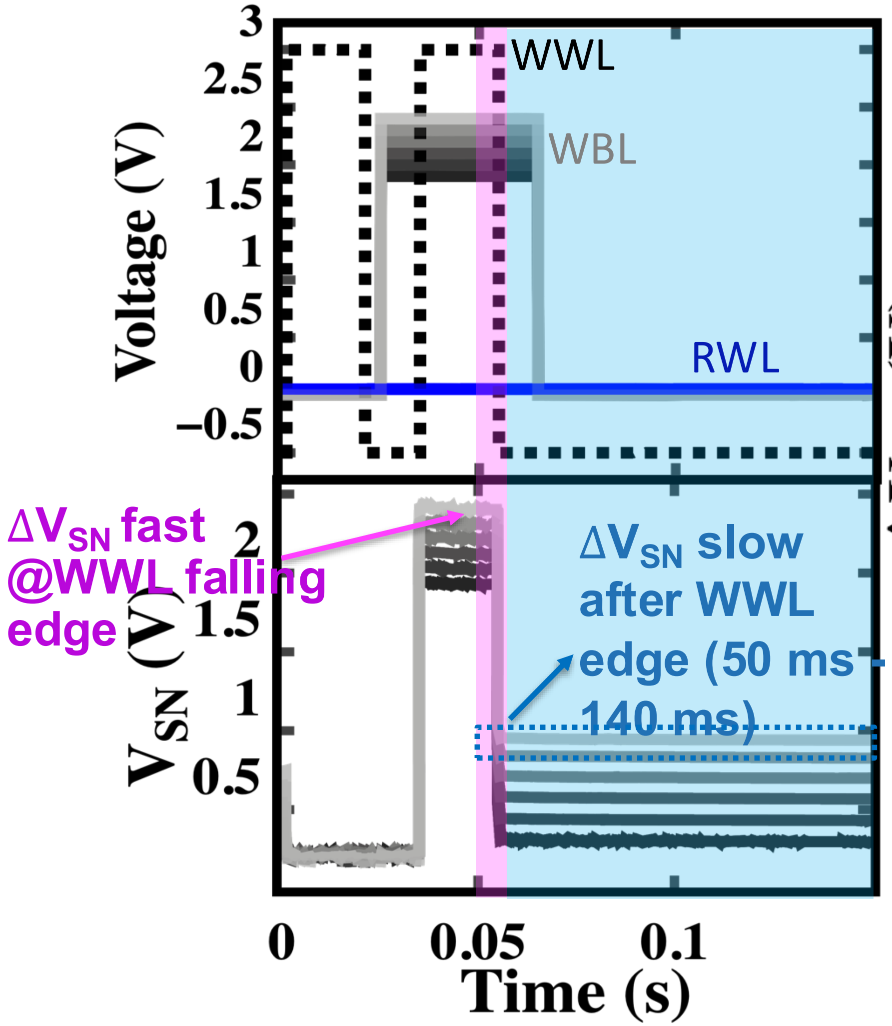


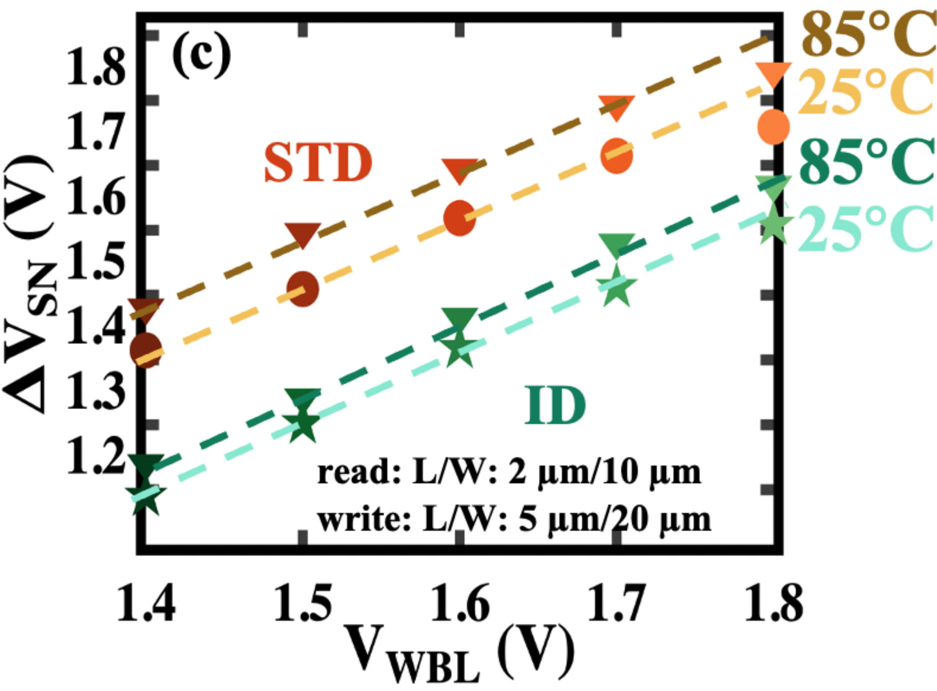


Dipole integration in OS Gain Cell memory

- V_{SN} drop reduced by ~13.5% at 85°C in ID GC
- Improved V_{SN} stability due to higher V_T



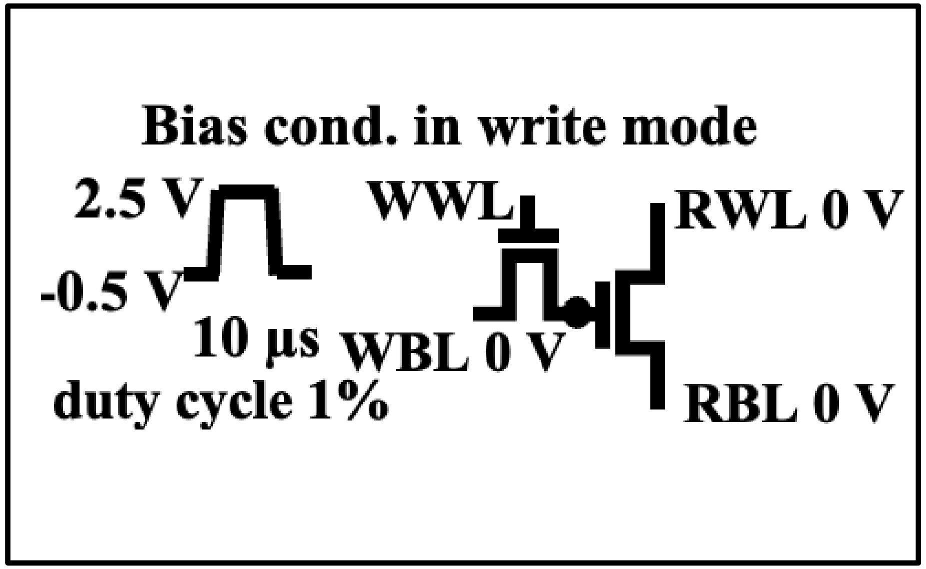


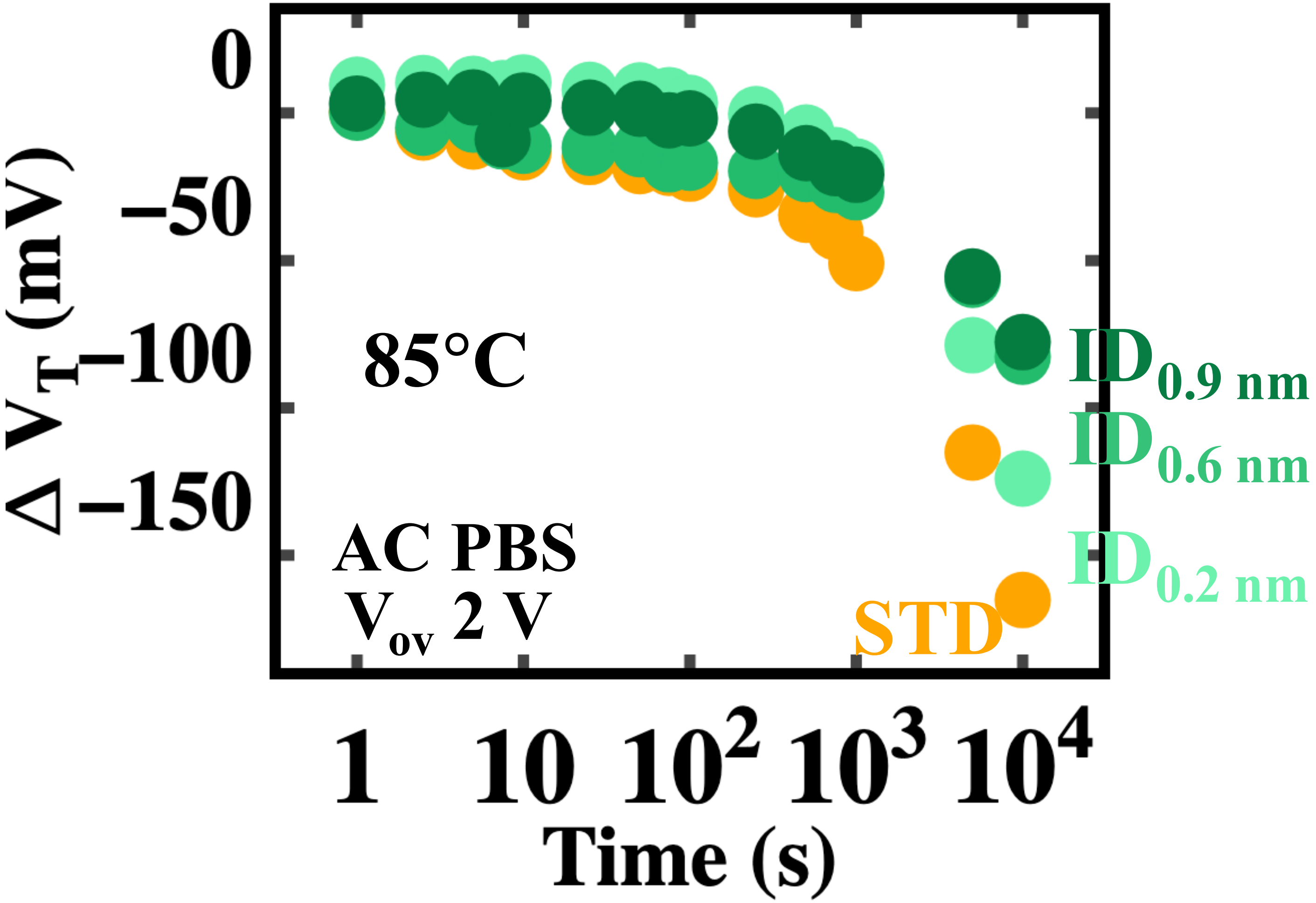


SN: storage node

AC/Pulsed PBS

- ID GC exhibits smaller shifts than the STD GC at 85°C

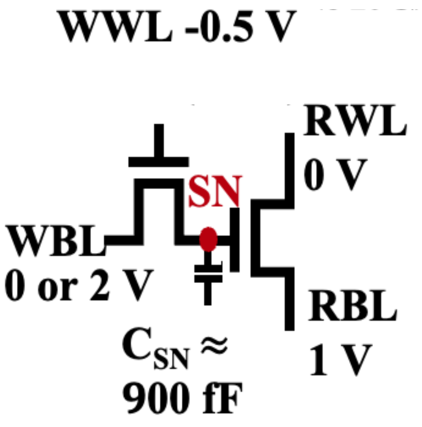


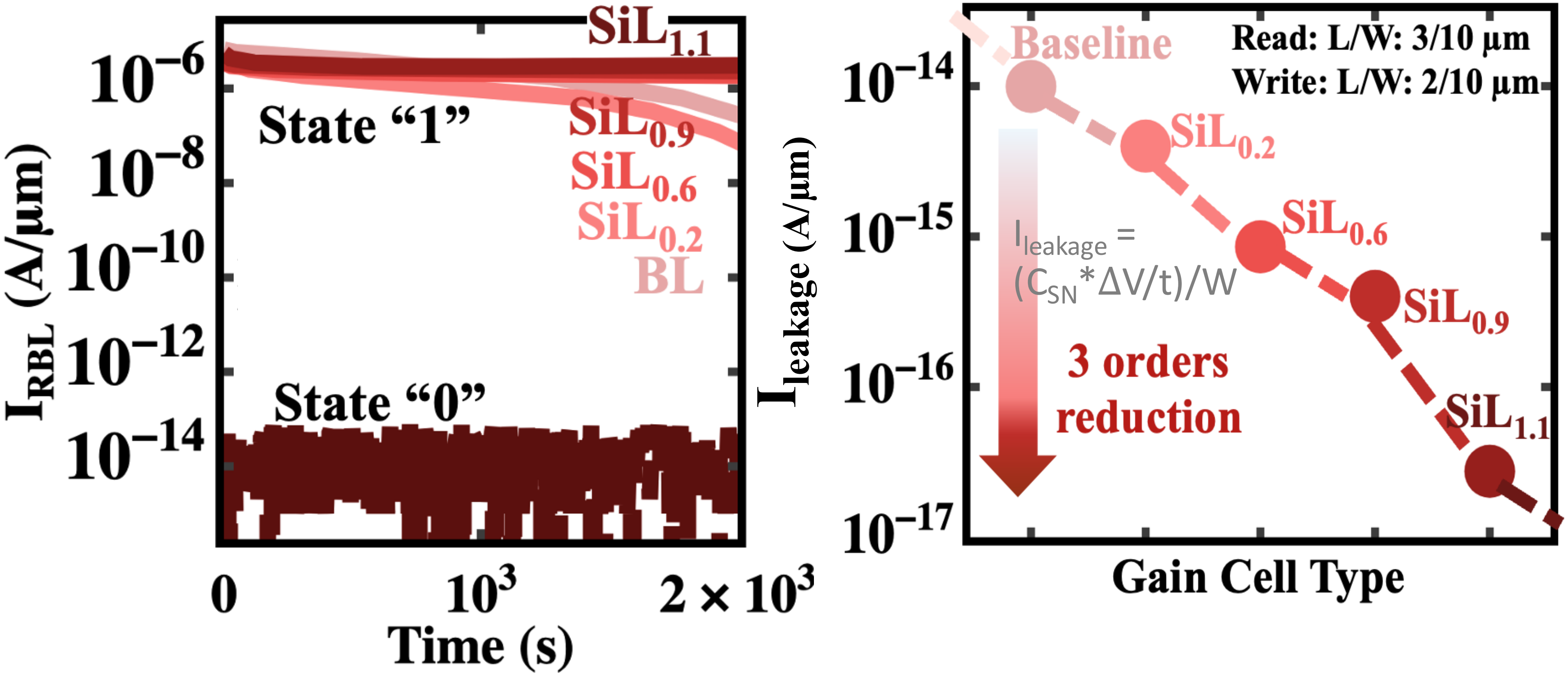


PBS: positive bias stress, GC: gain cell

Tunable Retention by ID Engineering: SiO_x dipole

- SiO_x dipole enables fine-grained multi-V_T and multi-retention capability



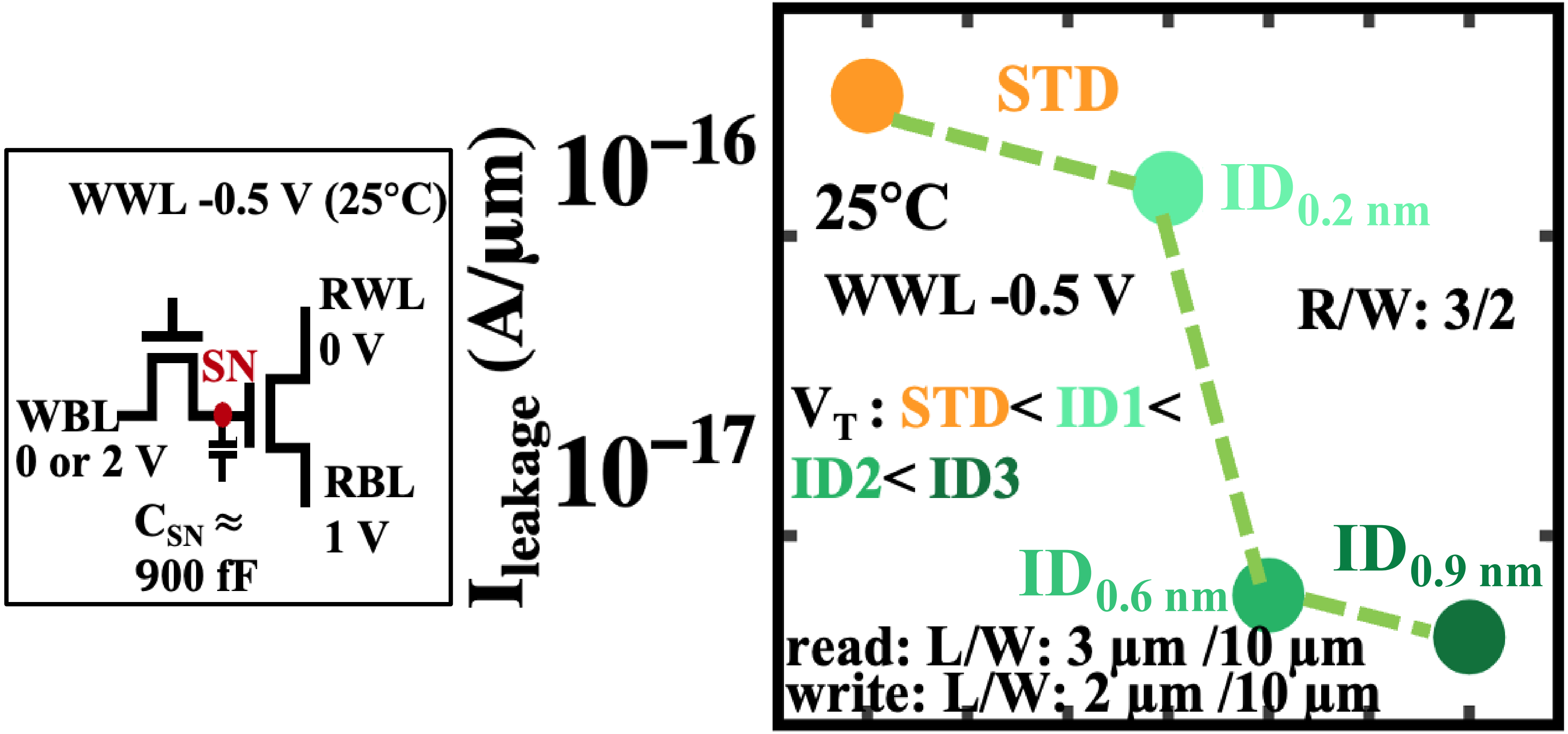


Keywords: CSN= storage node capacitance, ΔV= storage node voltage drop, t= retention time, W= width

F. F. Athena,.., H.-S. Philip Wong, *Nano Letters*, 2026

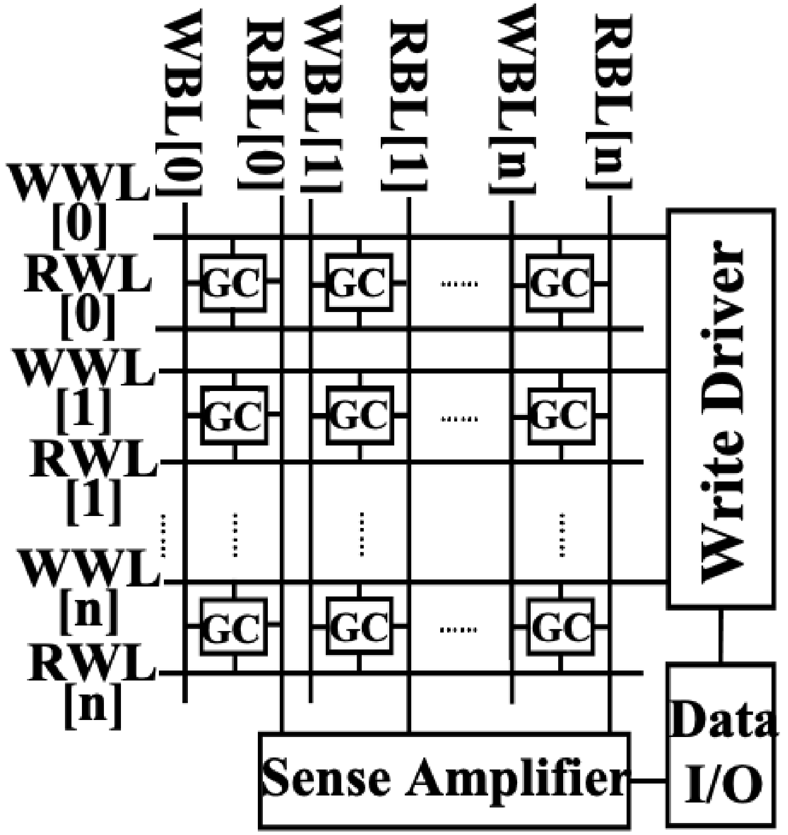
Tunable Retention by ID Engineering: AlO_x dipole

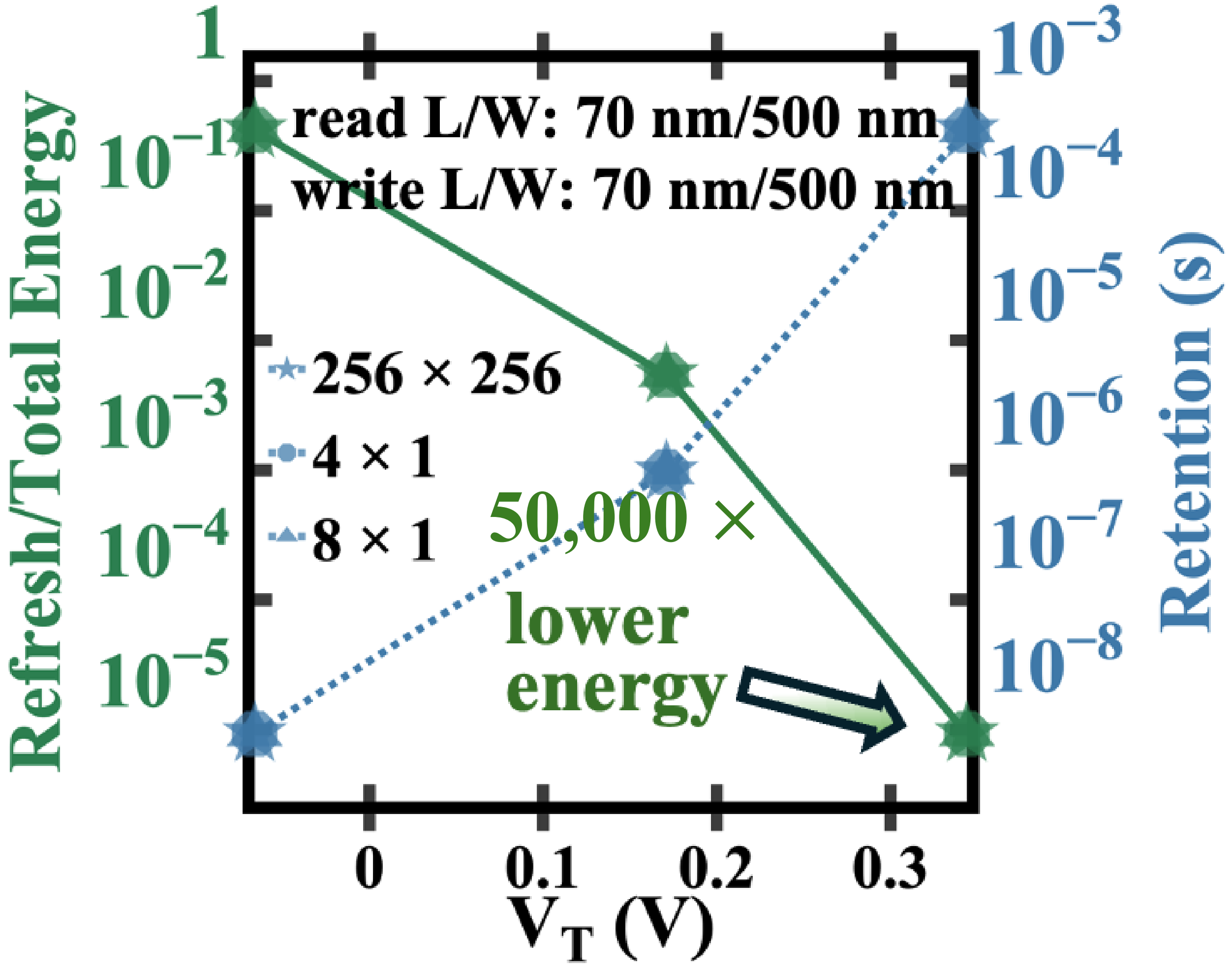
- As V_T increases, GC leakage reduces enabling longer retention
- ID3 GCs with various read/write sizes show excellent retention



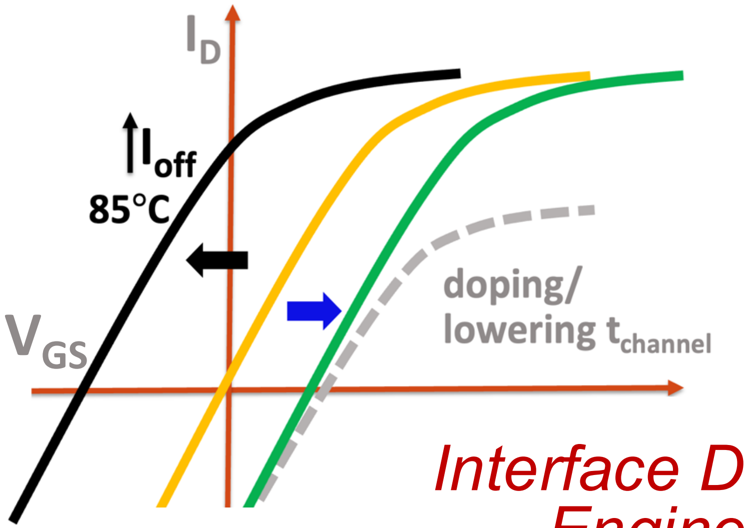
Dipole engineering of OS Gain Cell: Lower Refresh Power

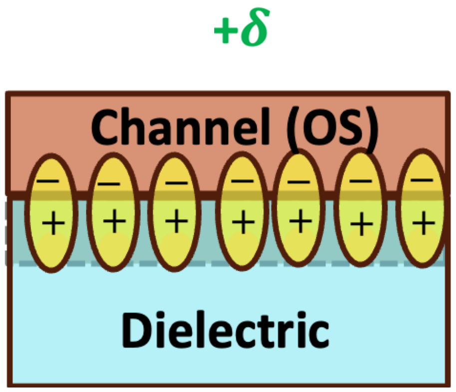
- High V_T GC reduces refresh cost
- 50,000 × lower energy consumption in high V_T GC than the baseline



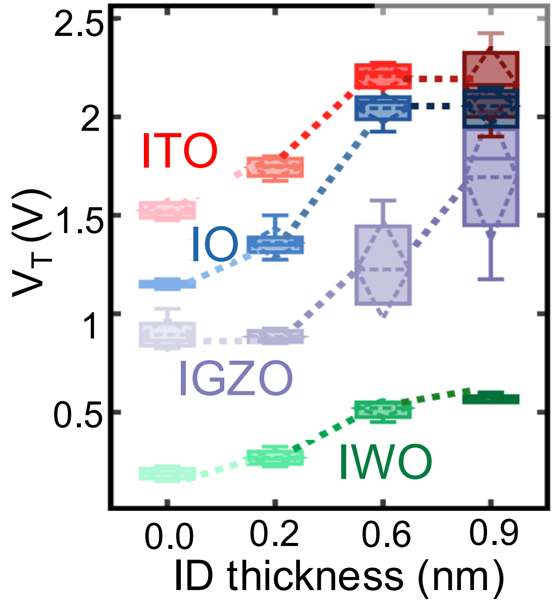


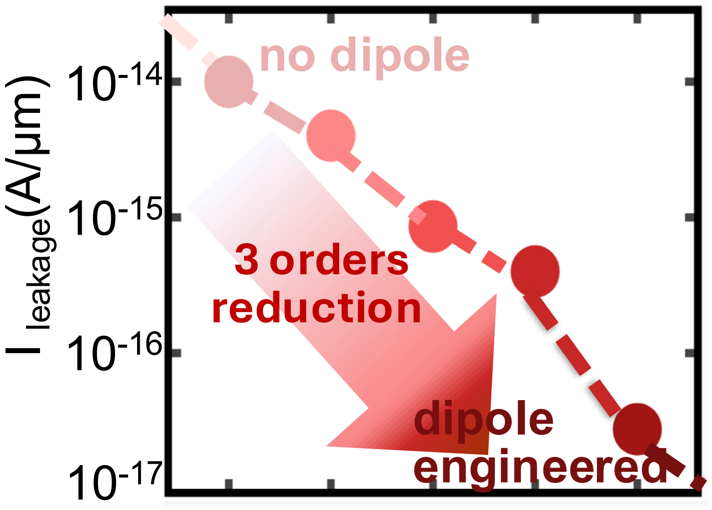
Interface Dipole Engineering for Tunable Retention





Interface Dipole (ID) Engineering





Keywords: IO: Indium Oxide, IWO: Indium Tungsten Oxide, ITO: Indium Tin Oxide, IGZO: Indium Gallium Zinc Oxide, V_T: Threshold Voltage

F. F. Athena,.., H.-S. Philip Wong, *VLSI Technology and Circuits*, 2025
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